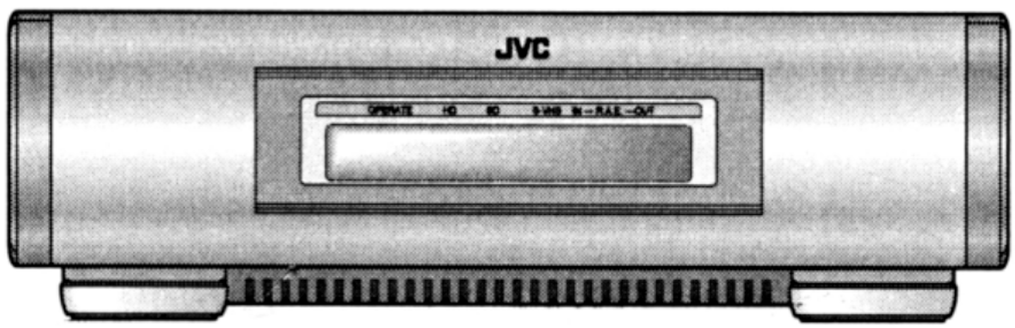
JVC

VIDEO TECHNICAL GUIDE

Hi-Vision VIDEO CASSETTE RECORDER

SR-W5U



Hi-Fi

S-VHS

W-VHS HD/SD

No. VTG82082
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SECTION 1
INTRODUCTION

1.1 DEVELOPMENT OF SR-W5U

In the past three years since the first model of W-VHS, SR-W320U was marketed, the high picture quality of the W-VHS has received wide acclaim in the market and has also been popular amongst users seeking high picture quality VCRs. The price of HR-W320U however does not allow many to enjoy the high picture quality of the W-VHS.
The SR-W5U was developed for users to enjoy the high picture quality of the W-VHS at close hand by further developing the high picture quality technologies of the SR-W320U and reducing costs by the rationalization of circuit configuration.

SECTION 2
NEW TECHNOLOGIES OF THE SR-W5U

2.1 HIGH QUALITY PICTURE ELEMENTAL TECHNOLOGIES

2.1.1 Precise two dimensional digital YC separation
Improvement of dot disturbances at the color boundaries of color character contours of still images which was difficult to implement in 3 dimensional YC separation has been implemented by the enhancement of edge part dynamic image detection system using a new edge detection method.

2.1.2 Three dimensional super color system
Improvement of the VCR color signal characteristics which has been long sought has been implemented by collecting color signals dispersed in the time axis direction and generating compensation signals by three dimensional signal processing. This has realized reproduction of detailed, and realistic color.

2.1.3 New 629 digital TBC
The 629 digital TBC mounted on the HR-20000 has been further improved.
In the past when tapes recording non-interlace non-standard signals such as video signals recorded from game machines were played by TBC ON, the images would sometimes become distorted.
By detecting non-standard signals and performing the appropriate solution, the new 629 digital TBC demonstrates high performance for a wider range of recorded tapes.

2.1.4 Wide range three dimensional Hadamard noise reduction
The three dimensional Hadamard noise reduction mounted on the SR-W320U has been further developed.
By improving the Hadamard conversion block dynamic range by 6 dB, noise reduction effects have been raised for noises generated at a wider area of signal change areas, thus expanding the effective range.

2.1.5 AI auto calibration
The performance of tapes is demonstrated to the full according to change in characteristics caused by changes in the video head with time and according to the tape to be recorded to detect and set the optimum recording level. Conventional models required one minute of calibration operations in order to perform accurate detection, but the SR-W5U is capable of high speed detection without sacrificing accuracy through the use of a new algorithm. It also displays detection results on the screen.

2.1.6 Dynamic distortion canceller
Due to the effects of distortion which occurs from the nonlinearity of hi-fi audio magnetic recording and playback systems, hi-fi audio chroma beats are generated during video playback. By electrically creating the distortion generated during hi-fi audio recording, superimposing with recording signals, and offsetting them during recording and playback, the hi-fi chroma crosstalk is reduced.

2.2 HIGH QUALITY SOUND ELEMENTAL TECHNOLOGIES

2.2.1 AI hyper tangent
Focusing on the fact that there exists zero cross pointS at which the tilt of signals at the start of compensation do not change during waveform interpolation, the current hyper tangent method has been further improved.

SECTION 3
W-VHS CIRCUIT

3.1 IMPROVEMENTS IN W-VHS CIRCUIT FROM SR-W320U

This section describes mainly the improvements of the SR-W5U from the SR-W320U.
For details of the fundamental technologies of the W-VHS circuit, refer to the Technical Guide for the SR-W320U.
The following shows the main improvements of the SR-W5U from the SR-W320U.

1) Simplification of circuits by deleting time axis expansion and compression processing
2) Improvement of response characteristics of jitter elimination by feed forward TBC
3) Automatic adjustment of playback clamp and enhancement of accuracy
4) Compatibility with special playbacks

The following describes each of the above improvement.

3.1.1 Simplification of circuits by deleting time axis expansion and compression processing and by integrating ICs

Fig. 3-1-1 shows the block diagram of the signal processing during the HD REC mode of the SR-W5U W-VHS circuit.

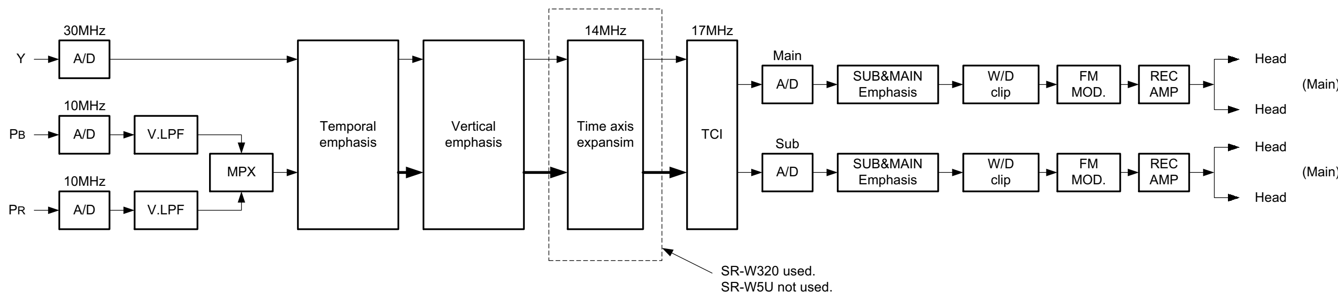


Fig. 3-1-1 Block Diagram of Signal Processing During W-VHS HD REC Mode

First take note that the SR-W320U incorporated the time axis expansion block between the vertical emphasis processing block and TCI processing block, while the SR-W5U omits this process.
In the SR-W320U, the signal processing speed of the IC performing TCI processing did not correspond to the clock frequency of the signal immediately after A/D conversion of the Y signal of the HD mode, and therefore the clock frequency of the signal was dropped by time axis expansion processing.
In the SR-W5U, the signal processing speed of the IC performing TCI processing has been made even higher so that TCI processing can be performed using the clock immediately after A/C conversion for the Y signal, thus eliminating the need for the time axis expansion processing. Consequently, the time axis compression processes (reverse processing) required during playback and the 14 MHz system clock circuit required for these processes can be eliminated.
At the same time, the number of ICs used for signal processing of the W-VHS has been reduced to two by integrating ICs.
This has as a result enabled sharp circuit simplification.

3.1.2 Improvement of response characteristics for jitter elimination by feed forward TBC

As shown in Fig. 3-1-2, the FF TBC system (Feed Forward System) generates several clocks with different phases using the multi-stage delay element from fixed clocks, and uses the clocks with the most matching phases for every one video signal line as the writing clocks for the A/D converter and memory to eliminate jitters.

As shown in Fig. 3-1-2, the characteristics of this method have outstanding response towards jitter components such as heads strike and skew by performing jitter correction independently for every H line.
Fig. 3-1-3 shows the block diagram of the FF TBC system of the SR-W5U.

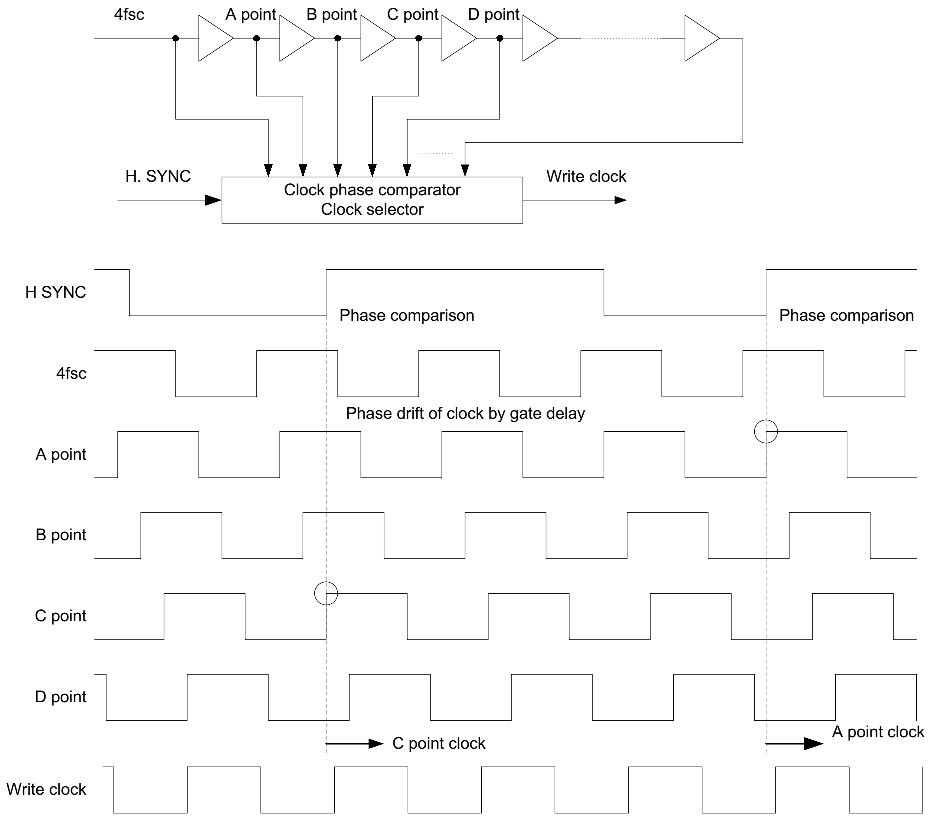


Fig. 3-1-2 Principle of Clock Generating Circuit

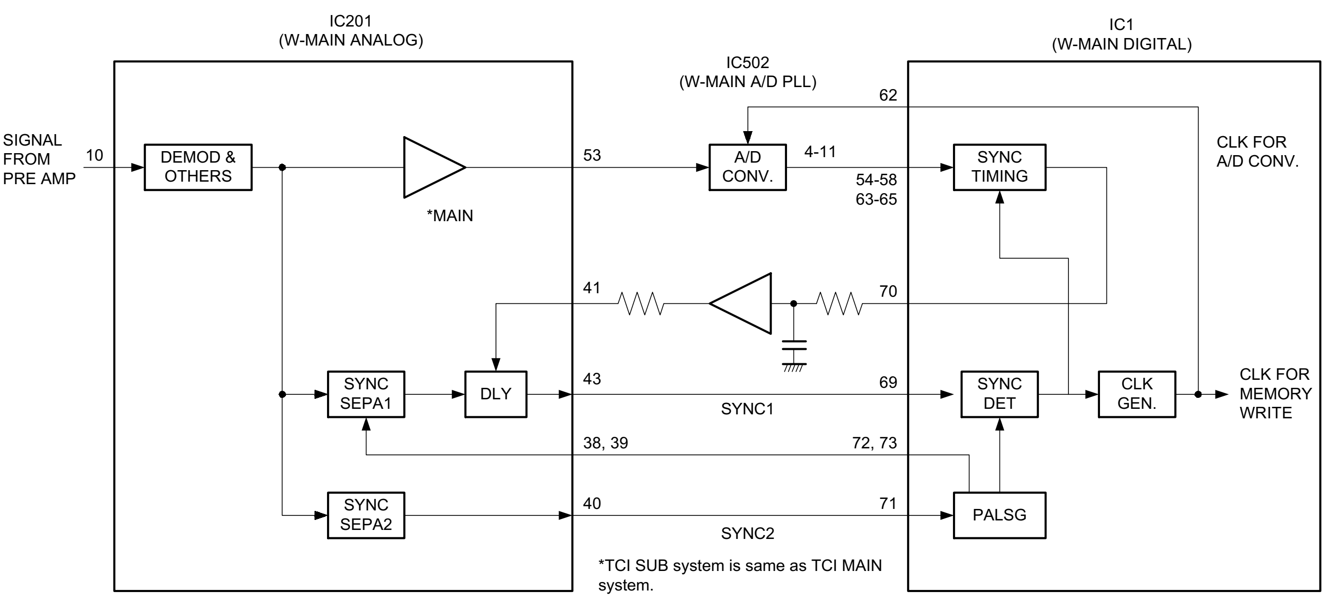


Fig. 3-1-3 Block Diagram of FF TBC System

The video signals are input to the SYNCSEPA1 and SYNCSEPA2.
SYNC1 is used mainly for the FF TBC while SYNC 2 is used as a spare for the partitioning of SYNC 1 and SYNCDET.
SYNC1 is detected by SYNCDET, and from amongst the clocks delayed by multiple stages from the CLKGEN at this timing, the clocks with the most matching phases are output, and are used as a write clock for the A/D converter and memory. However, in this block diagram (Fig. 3-1-3), the feedback group (DLY → SYNCDET → SYNCTIMING → DLY) which does not exist in the normal FF TBC system exists. This loop is a circuit which prevents deviation of phase between TCI signals with long change cycles and clocks caused by deviation of temperature characteristics of the signal system circuit and SYNC system circuit. This phase deviation is not displayed as jitter components on screens because of long cycles.
However, the problems described in the following may result from this phase deviation.
Assuming that phase deviation between a TCI signal with a long cycle and clock due to temperature characteristics of the circuit has occurred;
In this case, the starting point of the write clock and starting point of the signal have deviated as shown in Fig. 3-1-4. At the point of the playback TCI signal, the degree of phase deviation of Y and C is the same. However, with the playback TCI signal, as the C signal (R-Y, B-Y signal) has a higher compression rate than the Y signal, when it returns to the normal video signal, the phase deviation of the C signal becomes greater than that of the Y signal. For this reason, YC deviation occurs when it returns to the normal video signal.
This loop functions prevent YC deviation of the video signal as describes above.

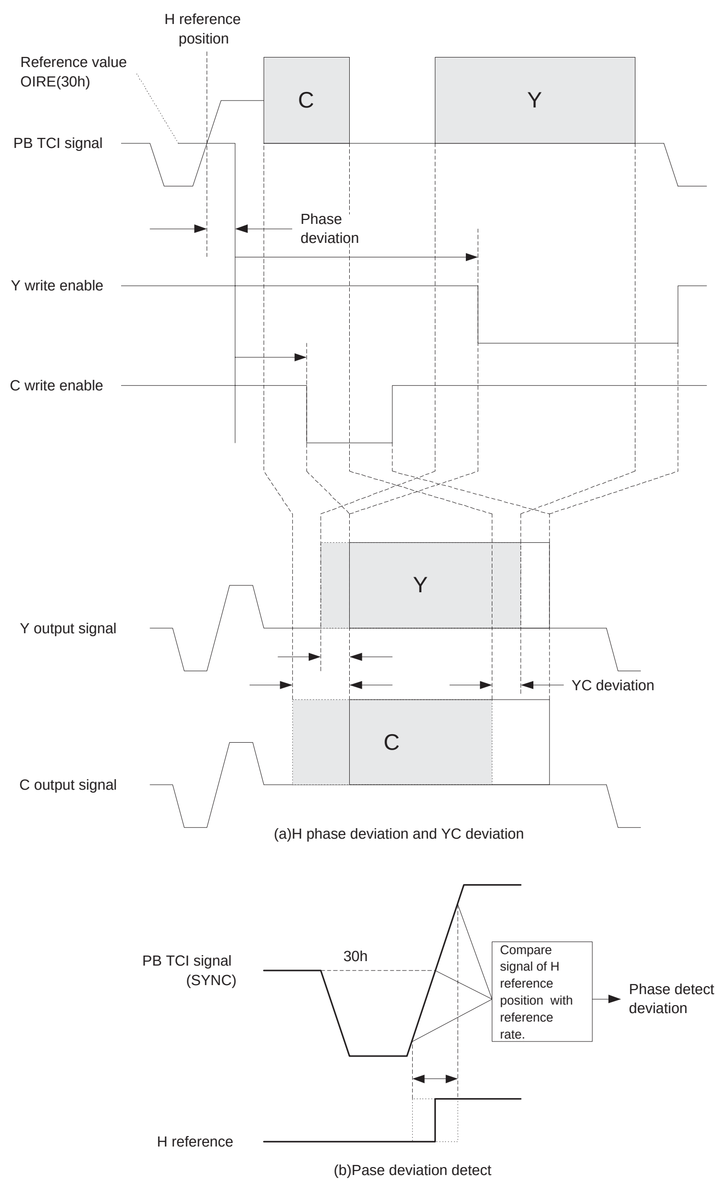


Fig. 3-1-4 Horizontal Phase Deviation

3.1.3 Automatic adjustment of playback clamp and accuracy improvement

Fig. 3-1-5 shows the method of detecting errors of the playback clamp system.

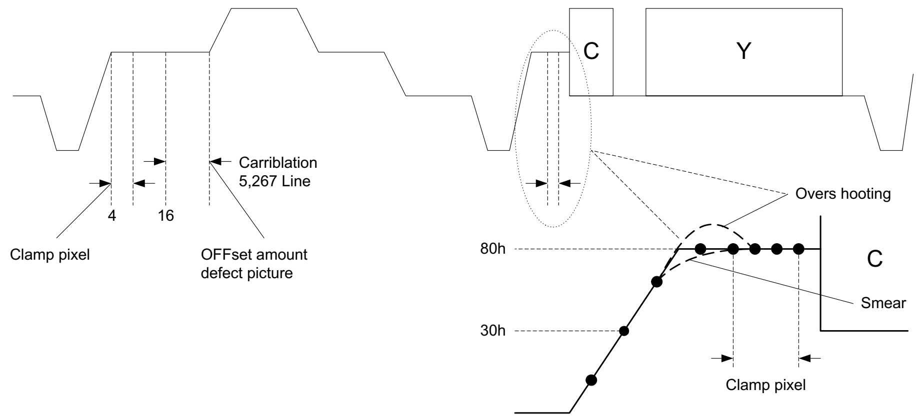


Fig. 3-1-5 Playback Clamp System Error Detection Method

In the SR-W320U, clamp errors were generated during playback due to overshooting and smearing caused by the main emphasis during recording and deemphasis during playback. This resulted in DC color shifting. As shown in Fig. 3-1-5, the SR-W5U adopts a method to calculate the clamp reference according to the offset amount detected from the difference between the clamp pixels and 50% white using the calibration signals of the TCI signal to correct this hue change and automatically correct change in the emphasis through the years and deviation of elements.
Fig. 3-1-6 shows the structure of the playback clamp system of the SR-W5U. The clamp reference value is calculated using a system controller software to reduce burden on the IC circuit and allow more freedom and expandability

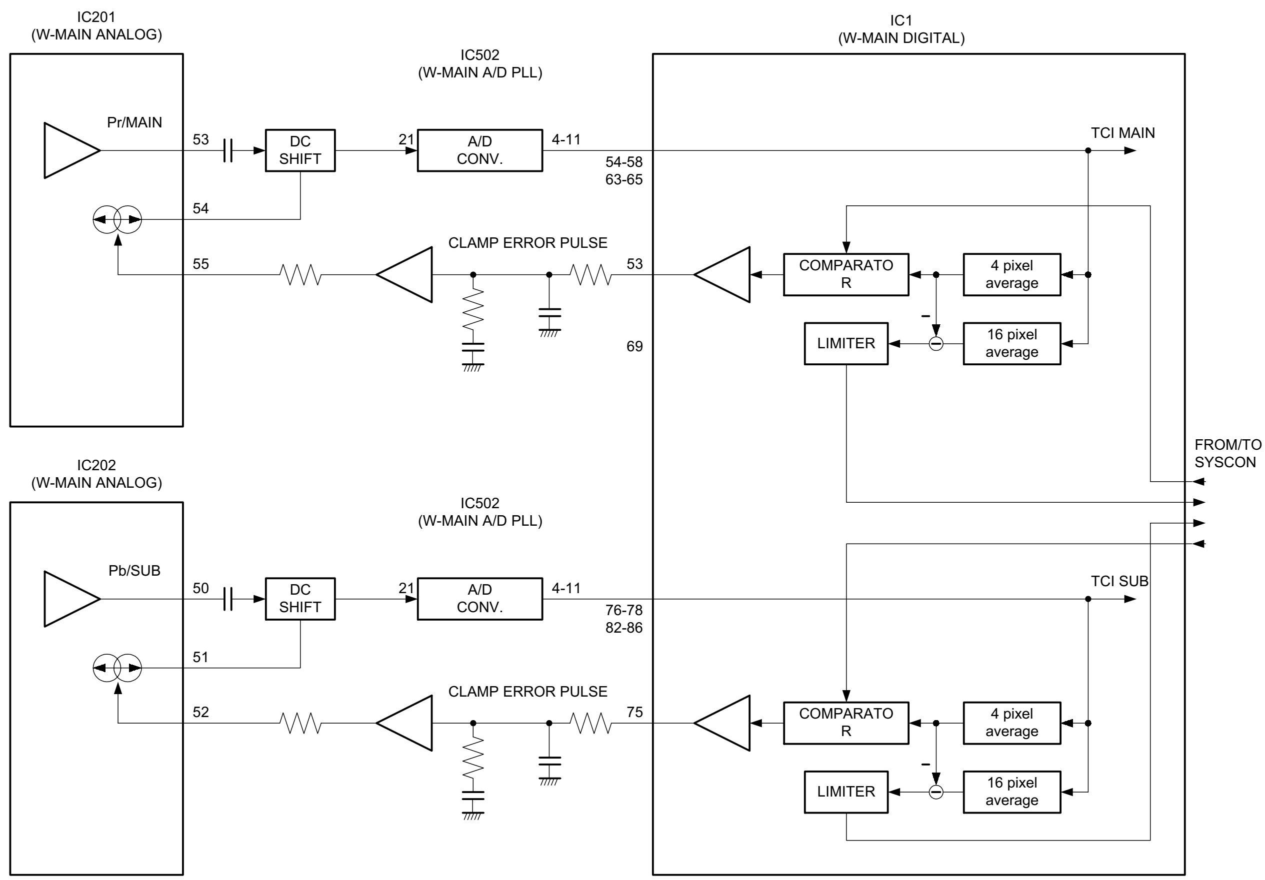


Fig. 3-1-6 Block Diagram of Playback Clamp System

3.1.4 Compatibility with special playback

As shown in Fig. 3-1-7, as the W-VCR is a 2-track parallel recording, it faces such problems as;it can only obtain intermittent playback output due to the guard band during search, and playback signals from one head exist.
During the still mode, because signals of one field cannot be obtained as shown in Fig. 3-1-7, slow playback by still intermittent feeding like VHS cannot be performed.

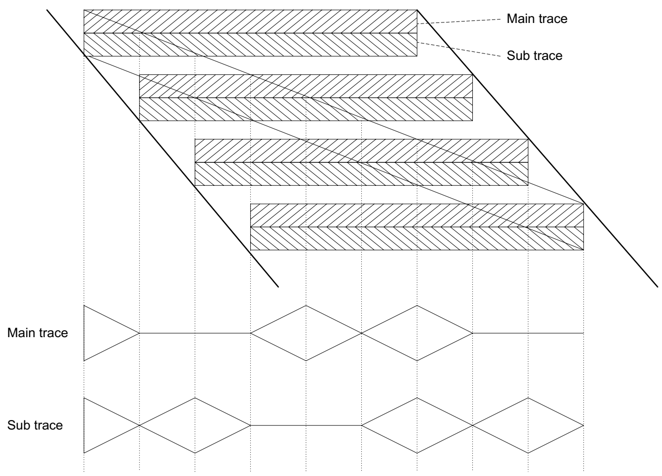


Fig. 3-1-7 Playback Output during Search

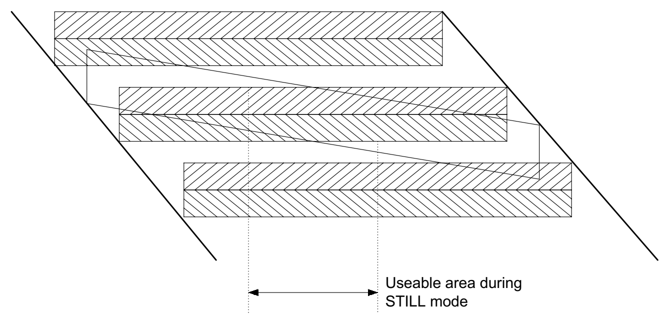


Fig. 3-1-8 Head Path during Still Mode

As W-VHS search is performed by rewriting of the memory, the tape speed must be set so that all information in the memory can be rewritten once periodically. This is shown in Fig. 3-1-9.
By logically analyzing the search speed and tape trace
pattern and setting the search speed to 2n±1/3 speed (n:integer), it has been clarified that rewriting of all information of the memory can be performed fixed, thus enabling various settings of the search speed. By using the playback signals of the reverse head and compensating the line, image movements have been made considerably smoother by tripping all video signals, thus realizing high speed search.
By adopting a method which inputs signal during scanning for the intermittent slow mode, intermittent slow by frame corresponding to the jog dial has also been realized.

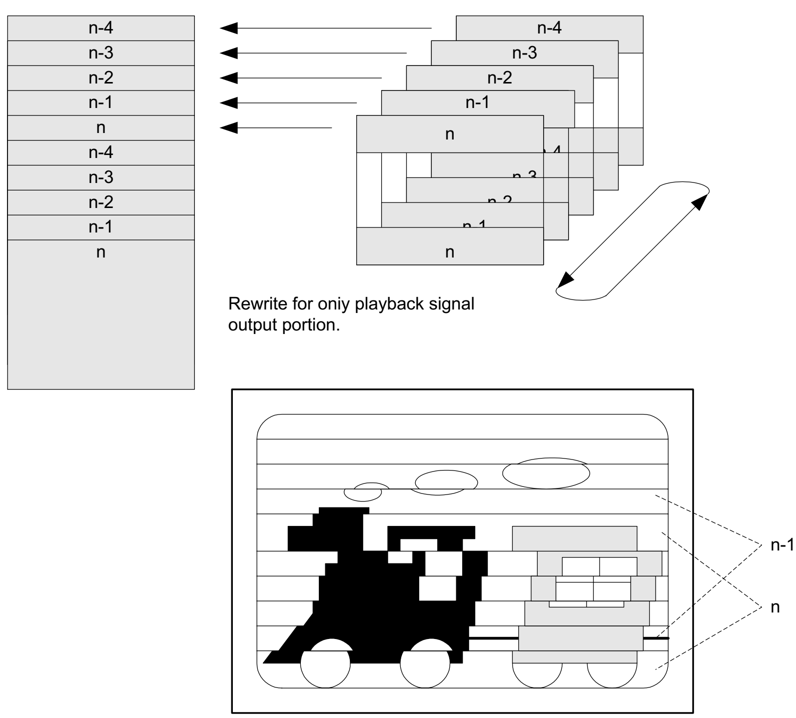


Fig. 3-1-9 Memory Rewriting and Video Output

3.2 W-VHS SIGNAL PROCESSING
3.2.1 Digital processing IC pin function
1. WPC IC (IC1) pin functions table (1/5)

Pin No.	Signal	In/Out	Description
1	GND	-	GND
2	GND	-	GND
3	FLRE1	Out	MBFLD Read Enable
4	FLWE1	Out	MBFLD Write Enable
5	SMC	In	Test Input (Normally "L")
6	CNTST	In	Test Input (Normally "L")
7	VBLK	Out	VBLK for OSD (common to TEST)
8	TMC1	In	Test Input (Normally "L")
9	TMC2	In	Test Input (Normally "L")
10	BUNRI	In	Test Input (Normally "L")
11	TEST	In	Test Input (Normally "L")
12	FLDA0	Out	Y in Rec or Sub FLD in PB Input Signal
13	FLDA1	Out	Y in Rec or Sub FLD in PB Input Signal
14	FLDA2	Out	Y in Rec or Sub FLD in PB Input Signal
15	FLDA3	Out	Y in Rec or Sub FLD in PB Input Signal
16	FLDA4	Out	Y in Rec or Sub FLD in PB Input Signal
17	FLDA5	Out	Y in Rec or Sub FLD in PB Input Signal
18	FLDA6	Out	Y in Rec or Sub FLD in PB Input Signal
19	FLDA7	Out	Y in Rec or Sub FLD in PB Input Signal
20	GND	-	GND
21	VDD	-	Power Input
22	AVDD	-	Analog Power for DA Input
23	NC	nc	NC
24	IOA	a	DA Ach Output
25	NC	nc	NC
26	IREF	a	Full-scale Current Adjustment for DA
27	NC	nc	NC
28	VREF	a	DA Reference Voltage
29	NC	nc	NC
30	COMP	a	Phase Compensation for DA
31	NC	nc	NC
32	IOB	a	DA Bch Output
33	NC	nc	NC
34	AGND	-	Analog GND for DA
35	NC	nc	NC
36	IOC	a	DA Cch Output
37	NC	nc	NC
38	AVDD	-	Analog Power for DA
39	MEMHL	In	Memory Control Polarity
40	VDD	-	Power Input
41	GND	-	GND
42	ADCK0	Out	Y CLK in REC
43	EAGCD	Out	AGC Error in REC
44	YCLP	Out	Y Clamp Error
45	ADAI7	In	Y AD Signal in REC
46	ADAI6	In	Y AD Signal in REC
47	ADAI5	In	Y AD Signal in REC
48	ADAI4	In	Y AD Signal in REC
49	ADAI3	In	Y AD Signal in REC
50	ADAI2	In	Y AD Signal in REC

Table 3-2-1 WPC IC (IC1) pin functions table (1/5)

- **WPC IC (IC1) pin functions table (2/5)**

Pin No.	Signal	In/Out	Description
51	ADAI1	In	Y AD Signal in REC
52	ADAI0	In	Y AD Signal in REC
53	RMCLP	Out	PR in Rec or Main Clamp Error in PB
54	ADBI7	In	PR in Rec or Main AD in PB
55	ADBI6	In	PR in Rec or Main AD in PB
56	ADBI5	In	PR in Rec or Main AD in PB
57	ADBI4	In	PR in Rec or Main AD in PB
58	ADBI3	In	PR in Rec or Main AD in PB
59	GND	-	GND
60	GND	-	GND
61	VDD	-	Power Input
62	ADCK1	Out	PR in Rec or Main Clock in PB
63	ADBI2	In	PR in Rec or Main AD in PB
64	ADBI1	In	PR in Rec or Main AD in PB
65	ADBI0	In	PR in Rec or Main AD in PB
66	CPMT	Out	EETCI Clamp Pulse
67	DOIMI	In	Main Dropout Signal
68	MEMVI	In	Main Envelop Signal
69	TMSYNCI	In	Main1stSync
70	MHDL	Out	Main 2nd Sync Delay Error
71	TMHS	In	Main 2nd Sync
72	MHP1	Out	Main 2nd Sync Separation Pulse
73	MHP0	Out	Main 2nd Sync Separation Pulse
74	SCK	In	Test Input (Normally "L")
75	BSCLP	Out	PB in Rec or Sub-clamp Error in PB
76	ADCI7	In	PB in Rec or Sub-AD in PB
77	ADCI6	In	PB in Rec or Sub-AD in PB
78	ADCI5	In	PB in Rec or Sub-AD in PB
79	ADCK2	Out	PB in Rec or Sub-clock in PB
80	GND	-	GND
81	VDD	-	Power Input
82	ADCI4	In	PB in Rec or Sub-AD in PB
83	ADCI3	In	PB in Rec or Sub-AD in PB
84	ADCI2	In	PB in Rec or Sub-AD in PB
85	ADCI1	In	PB in Rec or Sub-AD in PB
86	ADCI0	In	PB in Rec or Sub-AD in PB
87	DOISI	In	Sub Dropout Signal
88	SENVI	In	Sub Envelope Signal
89	TSSYNCI	In	Sub 1st Sync
90	SHDL	Out	Sub 2nd Sync Delay Error
91	TSHS	In	Sub 2nd Sync
92	SHP1	Out	Sub 2nd Sync Separation Pulse
93	SHP0	Out	Sub 2nd Sync Separation Pulse
94	EXTSYNC	In	Sync Signal for External Lock
95	BLK2	Out	Decoder BLK
96	VMASK	Out	V Mask Signal for SD Mode PLL
97	VPLLHS	Out	Frequency Divided Output for 30/28 MHz
98	VCO28N	In	28 MHz Clock Input
99	VXO28E	In	28 MHz Clock Input
100	VDD	-	Power Input

Table 3-2-1 WPC IC (IC1) pin functions table (2/5)

- **WPC IC (IC1) pin functions table (3/5)**

Pin No.	Signal	In/Out	Description
101	GND	-	GND
102	VXO30	In	30 MHz Clock Input
103	X14	In	14 MHz Clock Input
104	X28	In	28 MHz Clock Input
105	X30	In	30 MHz Clock Input
106	VCO17	In	17 MHz Clock
107	TPLLHS	Out	Frequency Divided Output for 17 MHz PLL
108	TPLLREF	Out	Reference Signal for 17 MHz PLL
109	MCLR	In	Master Clear
110	AMC	In	Test Input (Normally "L")
111	DCMRST	Out	Down Converter Memory Control
112	DCMWE	Out	Down Converter Memory Control
113	DCMRE	Out	Down Converter Memory Control
114	SVPBI7	In	SVP Output PR, PB Signal
115	SVPBI6	In	SVP Output PR, PB Signal
116	SVPBI5	In	SVP Output PR, PB Signal
117	SVPBI4	In	SVP Output PR, PB Signal
118	SVPBI3	In	SVP Output PR, PB Signal
119	SVPBI2	In	SVP Output PR, PB Signal
120	VDD	-	Power Input
121	GND	-	GND
122	GND	-	GND
123	SVPBI1	In	SVP Output PR, PB Signal
124	SVPBI0	In	SVP Output PR, PB Signal
125	SVPAI7	In	SVP Output Y Signal
126	SVPAI6	In	SVP Output Y Signal
127	SVPAI5	In	SVP Output Y Signal
128	SVPAI4	In	SVP Output Y Signal
129	SVPAI3	In	SVP Output Y Signal
130	SVPAI2	In	SVP Output Y Signal
131	SVPAI1	In	SVP Output Y Signal
132	SVPAI0	In	SVP Output Y Signal
133	AUXFBWE	Out	SVP PB AGC Position Signal
134	IMODECK	Out	SVP Control imodeck
135	IMODE	Out	SVP Control imode
136	SVPNO	Out	SVP Control SVP#
137	XRSTO	Out	SVP Control XRST
138	SVPMCK	Out	SVP MCK (17/3 MHz)
139	GND	-	GND
140	VDD	-	Power Input
141	IGFWRH	Out	SVP Control Igflga, Rstwh, Rstrh
142	WRE	Out	SVP Control WE, RE
143	SVPA0	Out	SVP Input Y Signal
144	SVPA1	Out	SVP Input Y Signal
145	SVPA2	Out	SVP Input Y Signal
146	SVPA3	Out	SVP Input Y Signal
147	SVPA4	Out	SVP Input Y Signal
148	SVPA5	Out	SVP Input Y Signal
149	SVPA6	Out	SVP Input Y Signal
150	SVPA7	Out	SVP Input Y Signal

Table 3-2-1 WPC IC (IC1) pin functions table (3/5)

- **WPC IC (IC1) pin functions table (4/5)**

Pin No.	Signal	In/Out	Description
151	SVPB0	Out	SVP Input PR, PB Signal
152	SVPB1	Out	SVP Input PR, PB Signal
153	SVPB2	Out	SVP Input PR, PB Signal
154	SVPB3	Out	SVP Input PR, PB Signal
155	SVPB4	Out	SVP Input PR, PB Signal
156	SVPB5	Out	SVP Input PR, PB Signal
157	SVPB6	Out	SVP Input PR, PB Signal
158	SVPB7	Out	SVP Input PR, PB Signal
159	SIEDGE	Out	SVP Effective Picture Elements Edge Signal
160	VDD	-	Power Input
161	GND	-	GND
162	SVENC	Out	SVP NTSC Modulation Signal
163	MPXR	Out	SVP PR Data Phase Pulse
164	MPXB	Out	SVP PB Data Phase Pulse
165	MPXQ	Out	SVP 9-Bit Data Phase Pulse
166	FRRST	Out	FRM Reset
167	FRRE4	Out	Y3FRM Read Enable
168	FRRE3	Out	Y2FRM Read Enable
169	FRRE2	Out	Y1FRM Read Enable
170	FRRE1	Out	PBRM Read Enable
171	FRRE0	Out	PRFRM Read Enable
172	FRWE4	Out	Y3FRM Write Enable
173	FRWE3	Out	Y2FRM Write Enable
174	FRWE2	Out	Y1FRM Write Enable
175	FRWE1	Out	PBFRM Write Enable
176	FRWE0	Out	PRFRM Write Enable
177	PBOE	Out	PB Odd/Even Signal
178	FRCK	Out	FRM Clock
179	GND	-	GND
180	GND	-	GND
181	VDD	-	Power Input
182	RECVS2O	Out	Recvssd 2 Output for SD2
183	PBOE2	In	PB Output Enable Input for SD2
184	RECVS2I	In	Recvssd 2 Input for SD2
185	HHD	Out	RGB Horizontal Drive
186	VVD	Out	RGB Vertical Drive
187	CCP	Out	RGB Clamp Pulse
188	BLK1	Out	RGB Horizontal Blanking
189	ADVV	Out	REF 30Hz for Servo
190	VSYNC	Out	REF 60Hz for Servo
191	MDFFI	In	Main DFF
192	SDFFI	In	Sub DFF
193	MOVEI	In	Tape Movement Signal in Slow Mode
194	SDCK	In	Serial Data Clock Input
195	ISD	In	Serial Data Input
196	SMODE	In	Serial Data Mode Signal
197	CS	In	System Control Data Enable
198	SDO	Out	Serial Data Output
199	FLWCK0	Out	SS, MBFLD Write Clock
200	GND	-	GND

Table 3-2-1 WPC IC (IC1) pin functions table (4/5)

- **WPC IC (IC1) pin functions table (5/5)**

Pin No.	Signal	In/Out	Description
201	VDD	-	Power Input
202	FLWE2	Out	BMFLD Write Enable
203	FLRSTW1	Out	RR, BMFLD Read Reset
204	FLRE0	Out	SSFLD Read Enable
205	FLDAI0	In	Sub in REC/Y FLD in PB Output Signal
206	FLDAI1	In	Sub in REC/Y FLD in PB Output Signal
207	FLDAI2	In	Sub in REC/Y FLD in PB Output Signal
208	FLDAI3	In	Sub in REC/Y FLD in PB Output Signal
209	FLDAI4	In	Sub in REC/Y FLD in PB Output Signal
210	FLDAI5	In	Sub in REC/Y FLD in PB Output Signal
211	FLDAI6	In	Sub in REC/Y FLD in PB Output Signal
212	FLDAI7	In	Sub in REC/Y FLD in PB Output Signal
213	FLRSTR1	Out	SS, BMFLD Read Reset
214	FLRE2	Out	BMFLD Read Enable
215	FLWE0	Out	SSFLD Write Enable
216	FLDB0	Out	PR, PB in REC/Main FLD in PB Input Signal
217	FLDB1	Out	PR, PB in REC/Main FLD in PB Input Signal
218	FLDB2	Out	PR, PB in REC/Main FLD in PB Input Signal
219	FLDB3	Out	PR, PB in REC/Main FLD in PB Input Signal
220	VDD	-	Power Input
221	GND	-	GND
222	FLWCK1	Out	BM, RRFLD Write Clock
223	FLDB4	Out	PR, PB in REC/Main FLD in PB Input Signal
224	FLDB5	Out	PR, PB in REC/Main FLD in PB Input Signal
225	FLDB6	Out	PR, PB in REC/Main FLD in PB Input Signal
226	FLDB7	Out	PR, PB in REC/Main FLD in PB Input Signal
227	FLWE3	Out	RRFLD Write Enable
228	FLRSTW0	Out	MB, SSFLD Read Reset
229	FLRSTR0	Out	MB, RRFLD Read Reset
230	FLRE3	Out	RRFLD Read Enable
231	FLDBI0	In	Main in REC/PR, PB FLD in PB Output Signal
232	FLDBI1	In	Main in REC/PR, PB FLD in PB Output Signal
233	FLDBI2	In	Main in REC/PR, PB FLD in PB Output Signal
234	FLDBI3	In	Main in REC/PR, PB FLD in PB Output Signal
235	FLDBI4	In	Main in REC/PR, PB FLD in PB Output Signal
236	FLDBI5	In	Main in REC/PR, PB FLD in PB Output Signal
237	FLDBI6	In	Main in REC/PR, PB FLD in PB Output Signal
238	FLDBI7	In	Main in REC/PR, PB FLD in PB Output Signal
239	FLRCK	Out	FLD Read Clock
240	VDD	-	Power Input

Table 3-2-1 WPC IC (IC1) pin functions table (5/5)

2. SVP IC (IC2) pin functions table (1/4)

Pin No.	Signal	In/Out	Description
1	DI6	In	WPC Output Y Signal
2	DI5	In	WPC Output Y Signal
3	DI4	In	WPC Output Y Signal
4	Vss	-	GND
5	DI3	In	WPC Output Y Signal
6	DI2	In	WPC Output Y Signal
7	DI1	In	WPC Output Y Signal
8	DI0	In	WPC Output Y Signal
9	VDD	-	Power Input
10	DSCKK	-	NC
11	DSOTO	-	NC
12	DSACK	-	NC
13	Vss	-	GND
14	TESTEN	-	NC
15	TESTRE	-	NC
16	TESTAK	-	NC
17	IGFLSA	In	Horizontal Sync (for Internal Processing)
18	IGFLSB	In	NTSC Color Select
19	XRST	In	SVP Reset Input
20	TESTRS	-	NC
21	INTREG	In	Interrupt (GND)
22	VDD	-	Power Input
23	SVP#0	In	SVP Bank Select (GND)
24	SVP#1	In	SVP Bank Select (VCC)
25	SVP#2	In	SVP Bank Select (GND)
26	IMODE	In	Mode Control
27	IMODECK	In	Mode Control Clock
28	Vss	-	GND
29	AUXDT	In	PB NR Control
30	AUXCK	In	PB NR Control Clock
31	TESTCK	In	Chip Test Clock (GND)
32	TESTMD	In	Chip Test MD (GND)
33	DO0	Out	WPC Input Y Signal
34	DO1	Out	WPC Input Y Signal
35	DO2	Out	WPC Input Y Signal
36	DO3	Out	WPC Input Y Signal
37	VDD	-	Power Input
38	DO4	Out	WPC Input Y Signal
39	DO5	Out	WPC Input Y Signal
40	DO6	Out	WPC Input Y Signal

Table 3-2-2 SVP IC (IC2) pin functions table (1/4)

- **SVP IC (IC2) pin functions table (2/4)**

Pin No.	Signal	In/Out	Description
41	DO7	Out	WPC Input Y Signal
42	DO8	Out	WPC Input PR/PB Signal
43	DO9	Out	WPC Input PR/PB Signal
44	DO10	Out	WPC Input PR/PB Signal
45	DO11	Out	WPC Input PR/PB Signal
46	Vss	-	GND
47	DO12	Out	WPC Input PR/PB Signal
48	DO13	Out	WPC Input PR/PB Signal
49	DO14	Out	WPC Input PR/PB Signal
50	DO15	Out	WPC Input PR/PB Signal
51	VDD	-	Power Input
52	DO16	Out	T.EMP Memory Input Y Signal
53	DO17	Out	T.EMP Memory Input Y Signal
54	DO18	Out	T.EMP Memory Input Y Signal
55	DO19	Out	T.EMP Memory Input Y Signal
56	DO20	Out	T.EMP Memory Input Y Signal
57	Vss	-	GND
58	AUXFBWE	In	PB AGC Timing
59	SRCK	In	DO Clock (30.24 MHz)
60	RSTRH	In	DO Horizontal Sync
61	RE	In	RE
62	OS	In	x2 Read-out (GND)
63	OE	In	DO Output Enable (VCC)
64	VDD	-	Power Input
65	DO21	Out	T.EMP Memory Input Y Signal
66	DO22	Out	T.EMP Memory Input Y Signal
67	DO23	Out	T.EMP Memory Input Y Signal
68	DO24	Out	T.EMP Memory Input PR/PB Signal
69	DO25	Out	T.EMP Memory Input PR/PB Signal
70	Vss	-	GND
71	DO26	Out	T.EMP Memory Input PR/PB Signal
72	DO27	Out	T.EMP Memory Input PR/PB Signal
73	DO28	Out	T.EMP Memory Input PR/PB Signal
74	DO29	Out	T.EMP Memory Input PR/PB Signal
75	VDD	-	Power Input
76	DO30	Out	T.EMP Memory Input PR/PB Signal
77	DO31	Out	T.EMP Memory Input PR/PB Signal
78	CR0	-	NC
79	CR1	-	NC
80	CR2	-	NC

Table 3-2-2 SVP IC (IC2) pin functions table (2/4)

- **SVP IC (IC2) pin functions table (3/4)**

Pin No.	Signal	In/Out	Description
81	CR3	-	NC
82	CR4	In	Test Input (VCC)
83	CR5	In	Test Input (VCC)
84	Vss	-	GND
85	CR6	In	Test Input (VCC)
86	CR7	In	Test Input (VCC)
87	TESTGU	-	NC
88	VDD	-	Power Input
89	CL7	-	NC
90	CL6	-	NC
91	CL5	-	NC
92	CL4	-	NC
93	Vss	-	GND
94	CL3	In	Test Input (VCC)
95	CL2	In	Test Input (VCC)
96	CL1	In	Test Input (VCC)
97	CL0	In	Test Input (VCC)
98	VDD	-	Power Input
99	VCORNG	In	PLL (VCC)
100	VCOIN	In	PLL (GND)
101	PFDOUT	In	PLL (VCC)
102	VDD	-	Power Input
103	MCK	In	Internal Clock (30.24 MHz)
104	PLL0	In	Internal PLL Multiplexer (VCC)
105	PLL1	In	Multiplexer Select (GND)
106	PLL2	In	X3(VCC)
107	Vss	-	GND
108	DI47	In	Color Phase Pulse
109	DI46	In	Color Phase Pulse
110	DI45	In	Color Phase Pulse
111	DI44	In	NTSC Color Phase Pulse
112	Vss	-	GND
113	DI43	In	EE Aperture Control
114	VLPF	In	Color VLPF Control
115	AGC	In	AGC Control
116	DI40	-	NC (VCC)
117	VDD	-	Power Input
118	DI39	-	NC (VCC)
119	DI38	-	NC (VCC)
120	DI37	-	NC (VCC)

Table 3-2-2 SVP IC (IC2) pin functions table (3/4)

- **SVP IC (IC2) pin functions table (4/4)**

Pin No.	Signal	In/Out	Description
121	DI36	-	NC (VCC)
122	DI35	-	NC (VCC)
123	DI34	-	NC (VCC)
124	DI33	-	NC (VCC)
125	DI32	-	NC (VCC)
126	Vss	-	GND
127	DI31	In	T.EMP Memory Output PR/PB Signal
128	DI30	In	T.EMP Memory Output PR/PB Signal
129	DI29	In	T.EMP Memory Output PR/PB Signal
130	DI28	In	T.EMP Memory Output PR/PB Signal
131	VDD	-	Power Input
132	DI27	In	T.EMP Memory Output PR/PB Signal
133	DI26	In	T.EMP Memory Output PR/PB Signal
134	DI25	In	T.EMP Memory Output PR/PB Signal
135	DI24	In	T.EMP Memory Output PR/PB Signal
136	DI23	In	T.EMP Memory Output Y Signal
137	Vss	-	GND
138	DI22	In	T.EMP Memory Output Y Signal
139	DI21	In	T.EMP Memory Output Y Signal
140	IS	In	DI x2 Speed Process (GND)
141	WE	In	DI Write Enable
142	RSTWH	In	DI Horizontal Sync
143	SWCK	In	DI Clock
144	VDD	-	Power Input
145	DI20	In	T.EMP Memory Output Y Signal
146	DI19	In	T.EMP Memory Output Y Signal
147	DI18	In	T.EMP Memory Output Y Signal
148	DI17	In	T.EMP Memory Output Y Signal
149	DI16	In	T.EMP Memory Output Y Signal
150	Vss	-	GND
151	DI15	In	WPC Output PR/PB Signal
152	DI14	In	WPC Output PR/PB Signal
153	DI13	In	WPC Output PR/PB Signal
154	DI12	In	WPC Output PR/PB Signal
155	VDD	-	Power Input
156	DI11	In	WPC Output PR/PB Signal
157	DI10	In	WPC Output PR/PB Signal
158	DI9	In	WPC Output PR/PB Signal
159	DI8	In	WPC Output PR/PB Signal
160	DI7	In	WPC Output Y Signal

Table 3-2-2 SVP IC (IC2) pin functions table (4/4)

3.2.2 HD REC mode signal processing

The signal processing of the HD REC mode of the W-VHS circuit can broadly be divided into the analog processing circuit composed mainly of IC201 and IC202, and the digital processing circuit composed of mainly IC1 and IC2. Input signals are set to the appropriate level and frequency band, subjected to digital processing, and finally modulated in the analog processing circuit and recorded on tape.

In the HD REC mode, the Y, Pb, and Pr signals are input to the W I/O board and subject to AGC and filtering processes in IC201 and IC202. Each signal is then A/D converted by a specific clock respectively and sent to the digital processor. After this, the Y signal is directly subjected to digital processing, but the Pb and Pr signals are first subjected to multiplexing by the MPX block of IC1. Multiplexing is the process by which the Pb and Pr signals sent by the two lines shown in Fig. 3-2-1 are clock-increased, and sent by one line by time division processing.

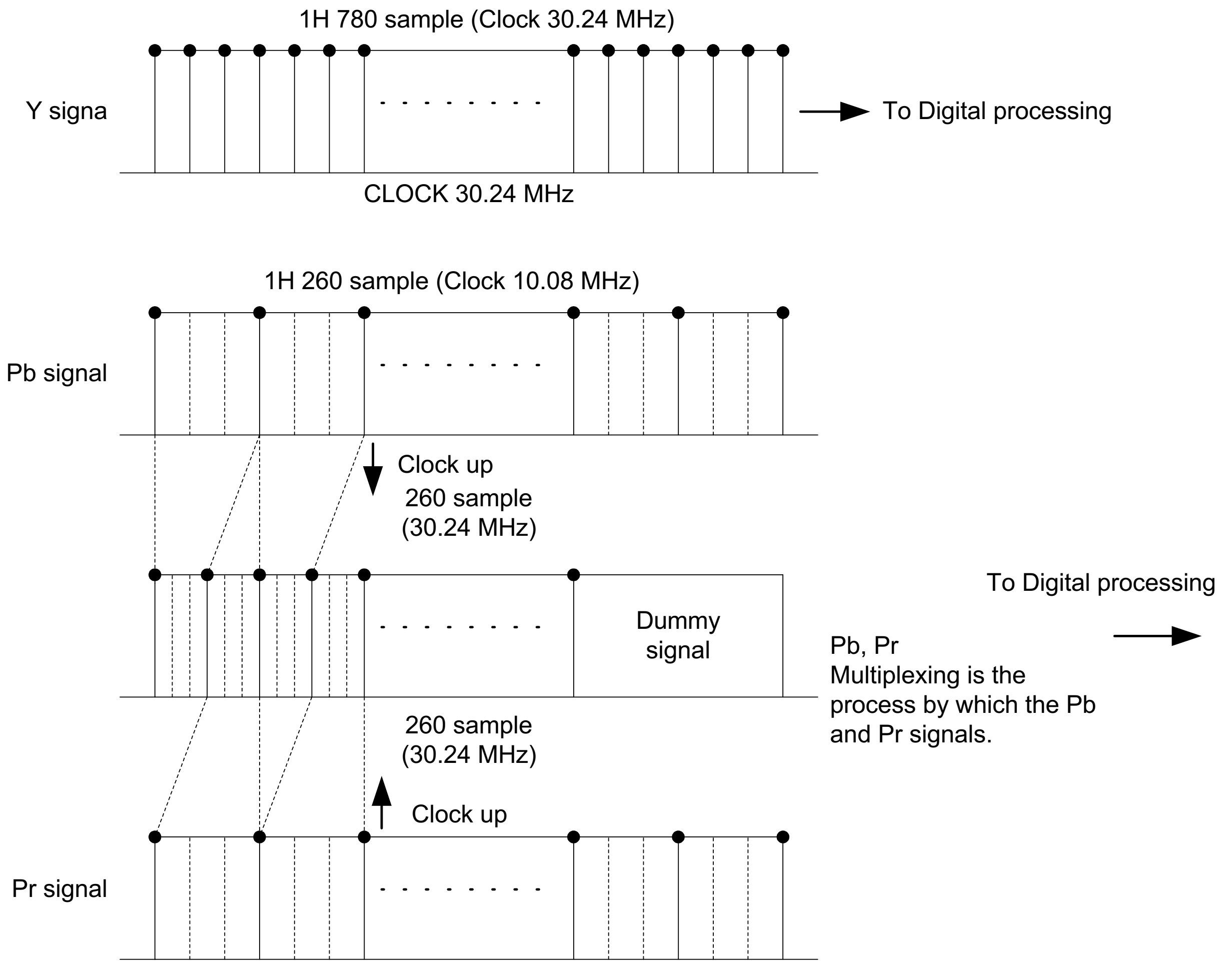


Fig. 3-2-1 Multiplexing of Pb and Pr Signals

The Y signals and Pb and Pr signals subjected to multiplexing are subjected to temporal emphasis and vertical emphasis processing in IC2, and become the TCI signal by TCI processing in IC1 later on. This TCI signal is then subjected to emphasis and FM modulation processing in IC201, and recorded on tape.

- HD REC mode signal processing (1/4)

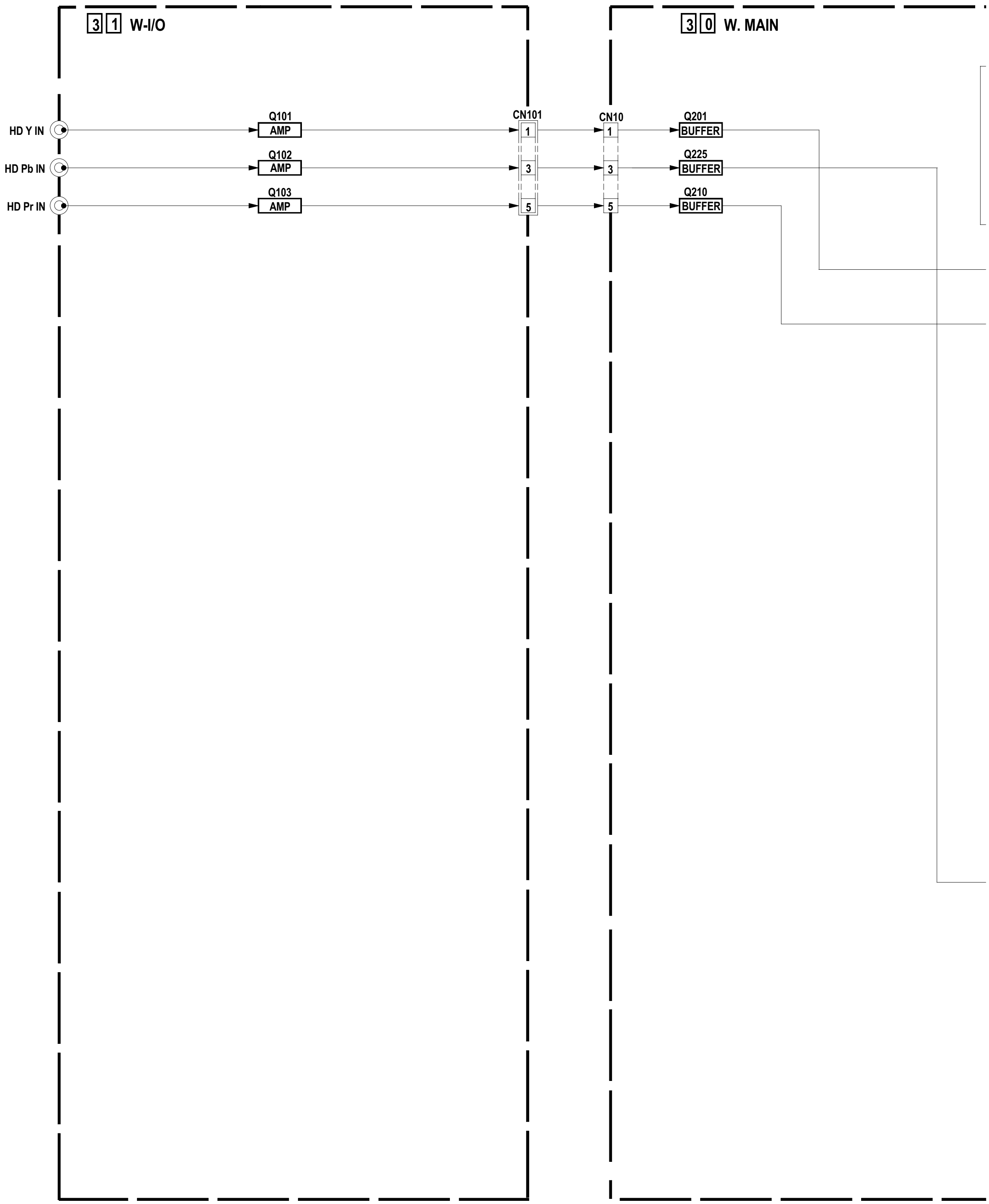


Fig. 3-2-2 Block Diagram of HD REC Mode Signal Processing (1/4)

• **HD REC mode signal processing (2/4)**

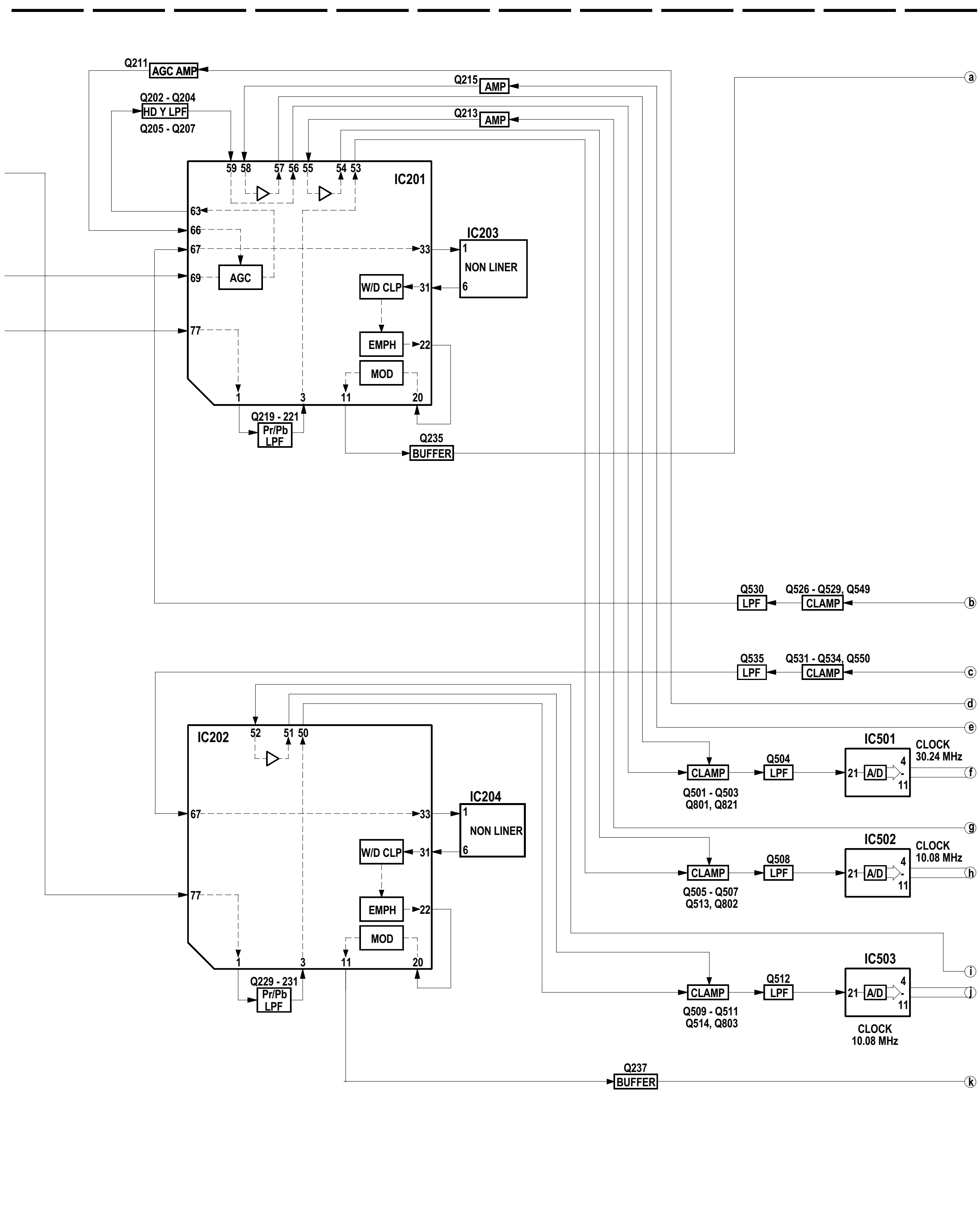


Fig. 3-2-2 Block Diagram of HD REC Mode Signal Processing (2/4)

• **HD REC mode signal processing (3/4)**

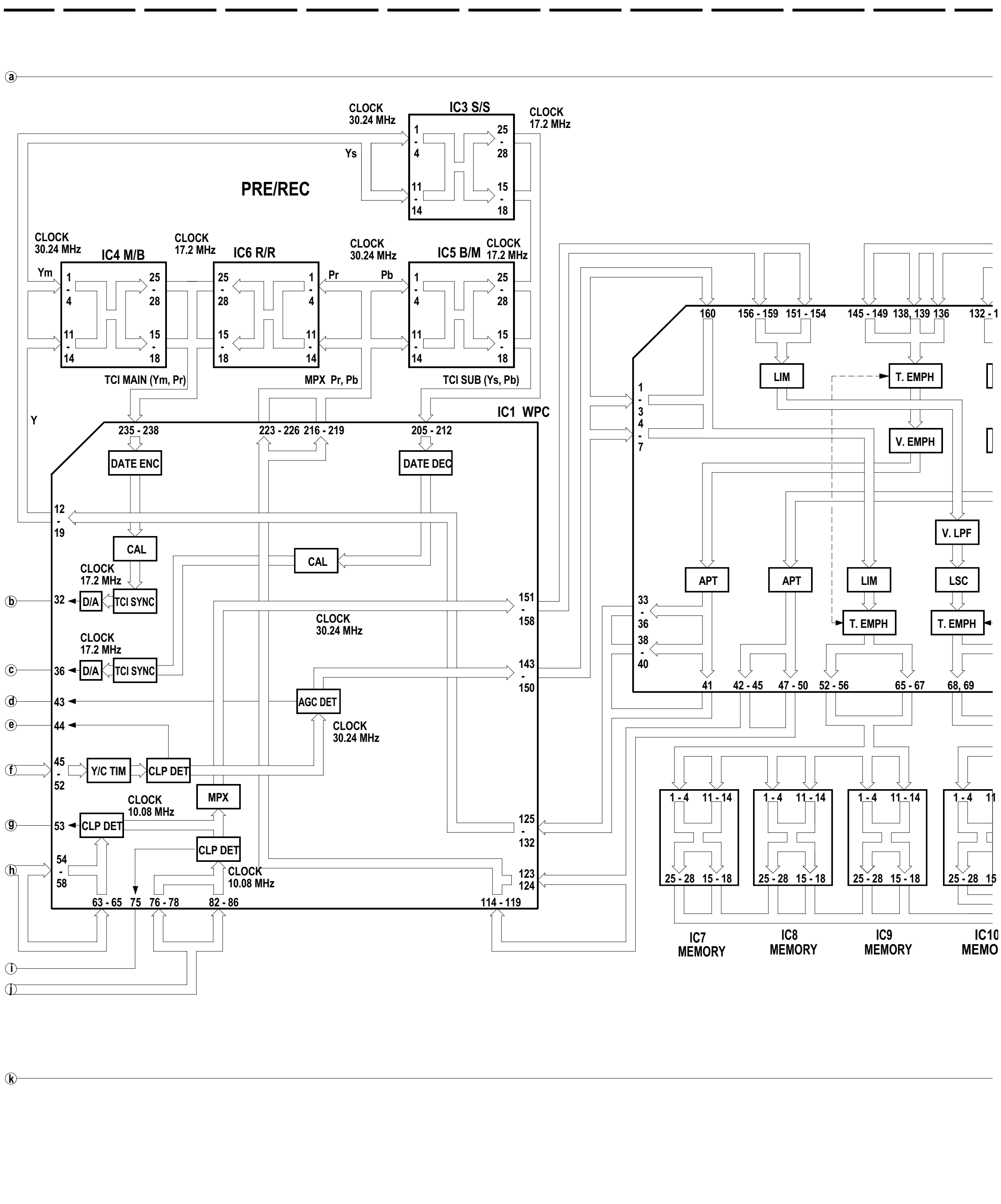


Fig. 3-2-2 Block Diagram of HD REC Mode Signal Processing (3/4)

• **HD REC mode signal processing (4/4)**

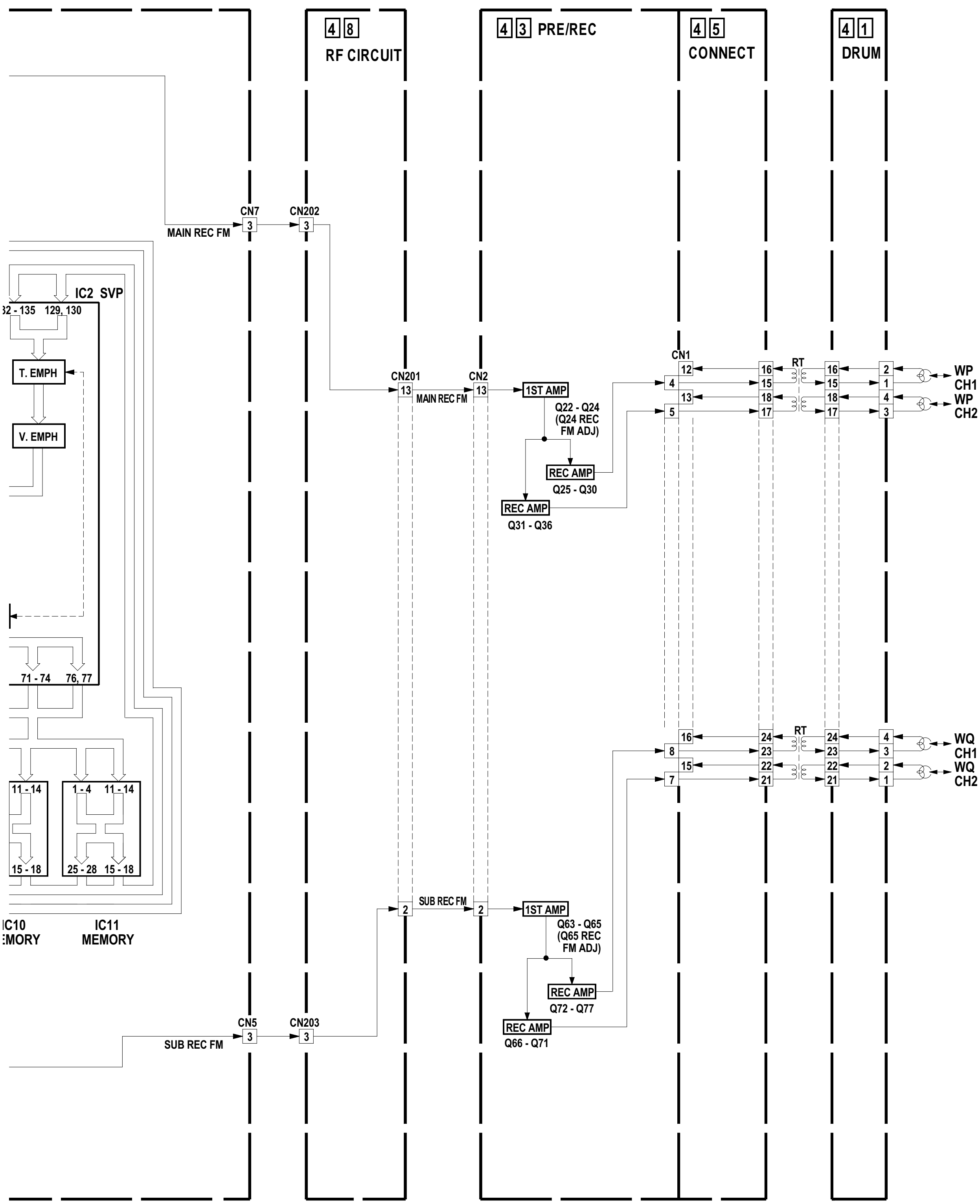


Fig. 3-2-2 Block Diagram of HD REC Mode Signal Processing (4/4)

3.2.3 HD PB MODE SIGNAL PROCESSING

In the signal processing of the HD PLAY mode, the process totally opposite to the signal processing of the HD REC mode is performed.

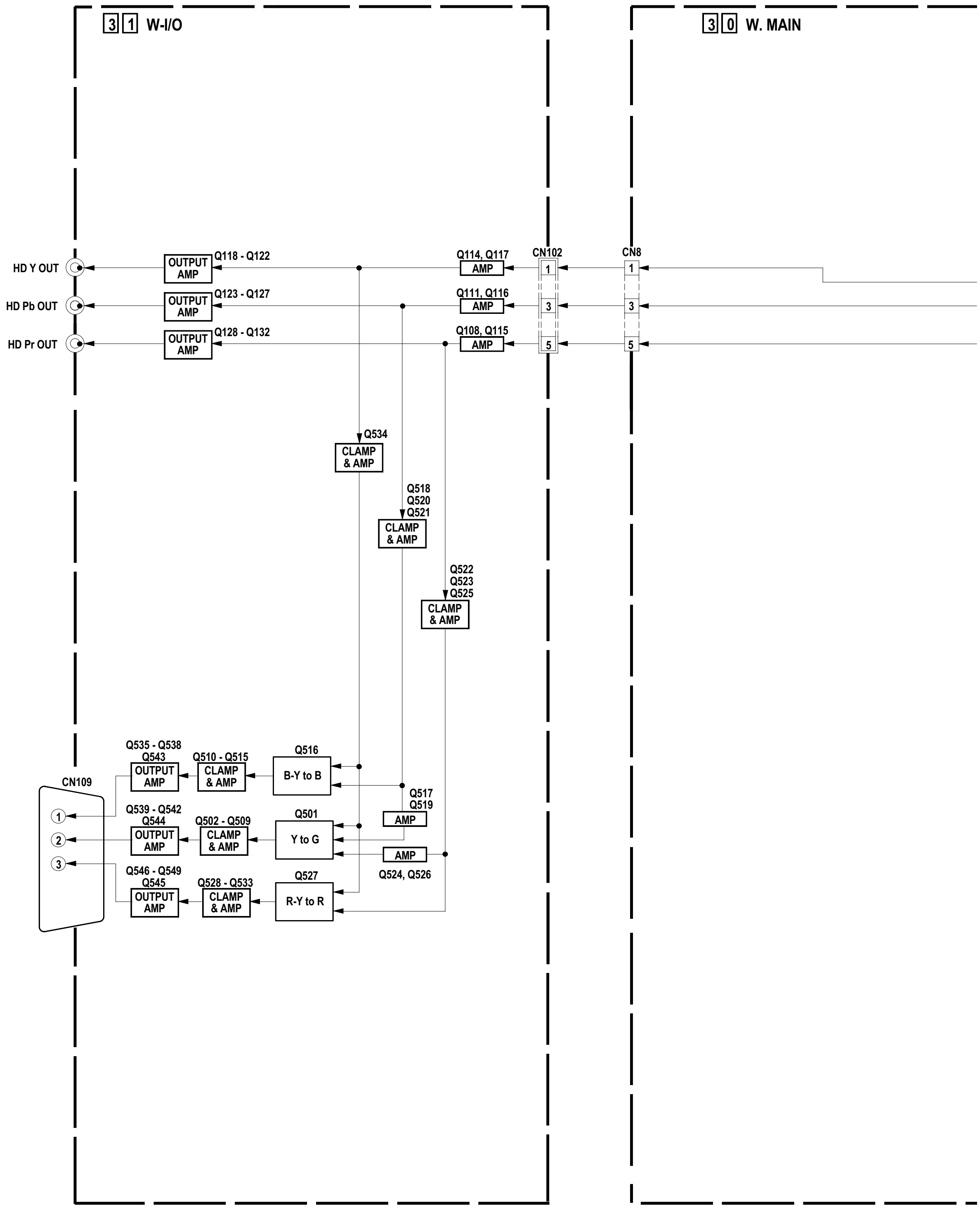


Fig. 3-2-3 Block Diagram of HD PB Mode Signal Processing (1/4)

• **HD PB mode signal processing (2/4)**

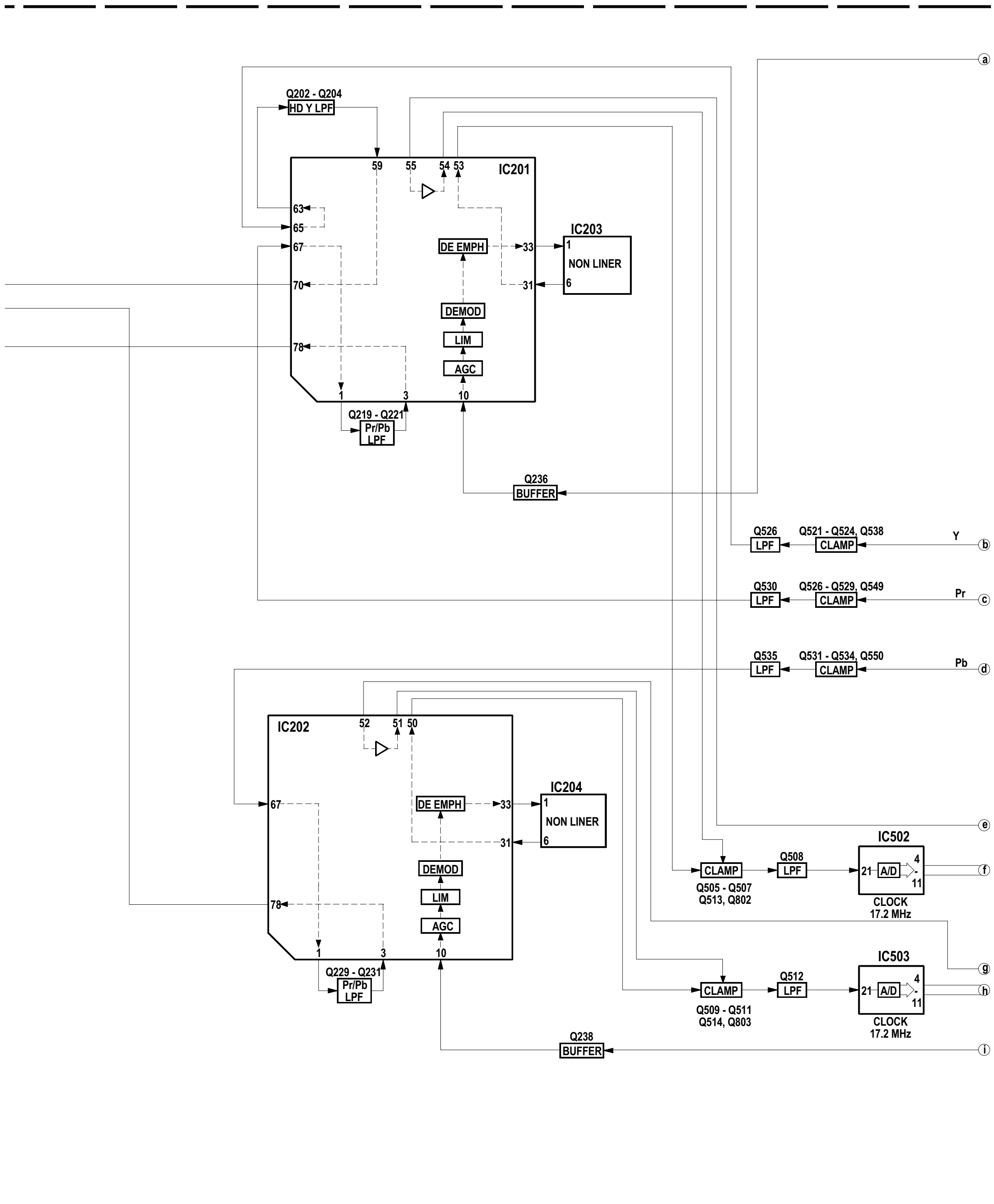


Fig. 3-2-3 Block Diagram of HD PB Mode Signal Processing (2/4)

• **HD PB mode signal processing (3/4)**

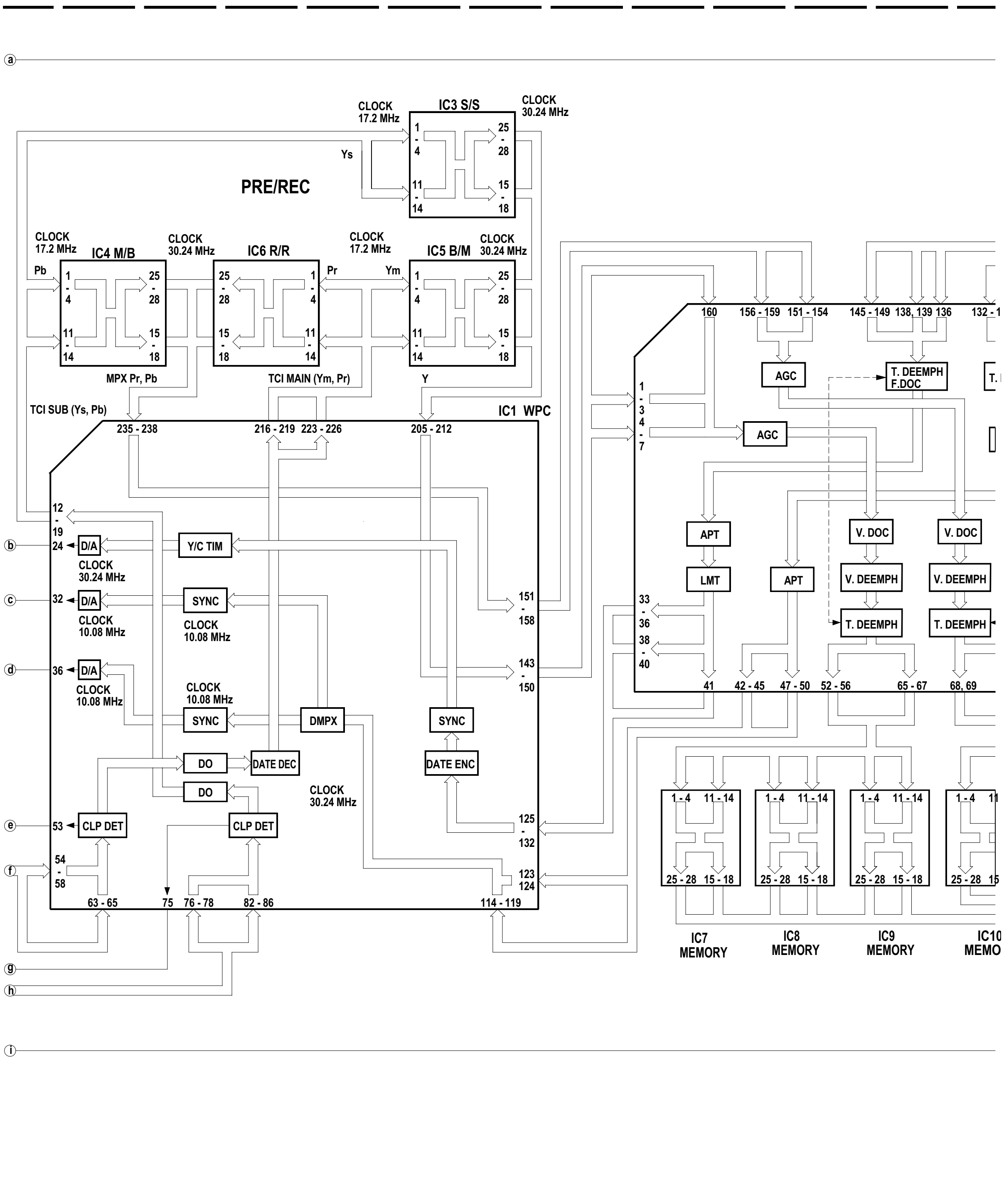


Fig. 3-2-3 Block Diagram of HD PB Mode Signal Processing (3/4)

• **HD PB mode signal processing (4/4)**

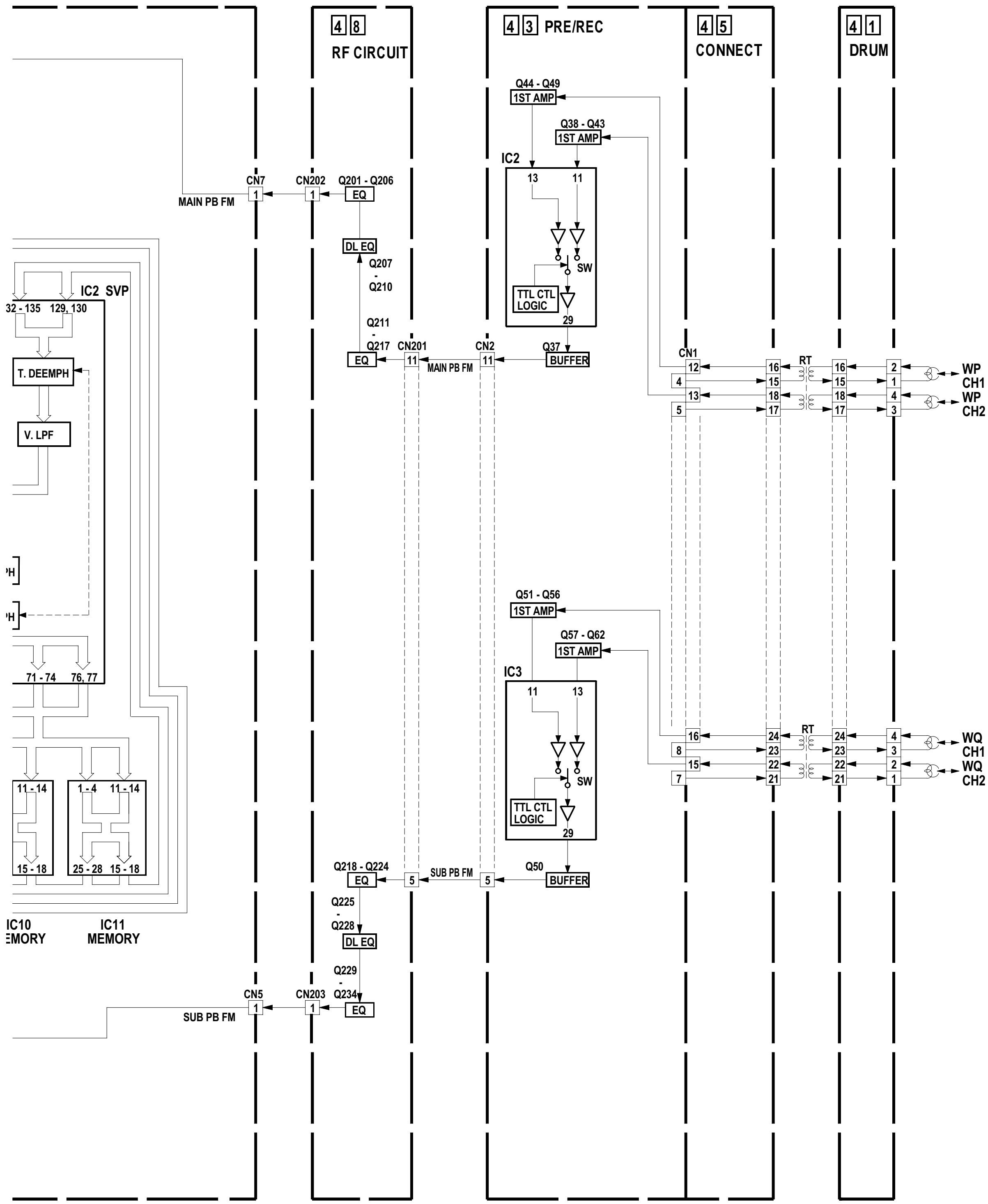


Fig. 3-2-3 Block Diagram of HD PB Mode Signal Processing (4/4)

3.2.4 SD REC MODE SIGNAL PROCESSING

The signal processing of the SD REC mode is basically the same as that of the HD REC mode. But as shown in Fig. 3-2-4, the frequency, etc. of clocks change because NTSC signals are processed. In the SD REC mode, as Y and C signals are input, the chroma encoder (IC701) becomes necessary immediately after input.

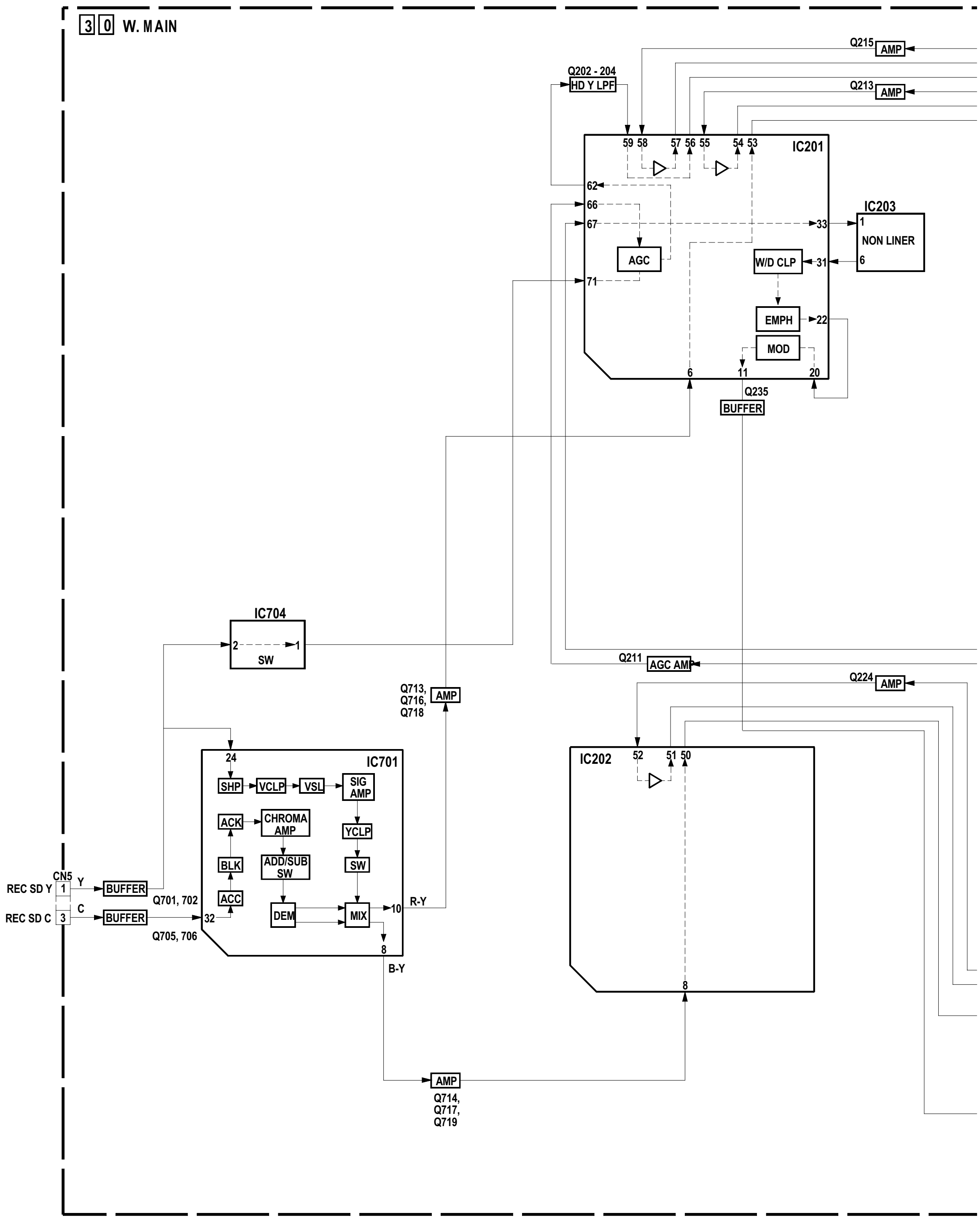


Fig. 3-2-4 Block Diagram of SD REC Mode Signal Processing (1/4)

• **SD REC mode signal processing (2/4)**

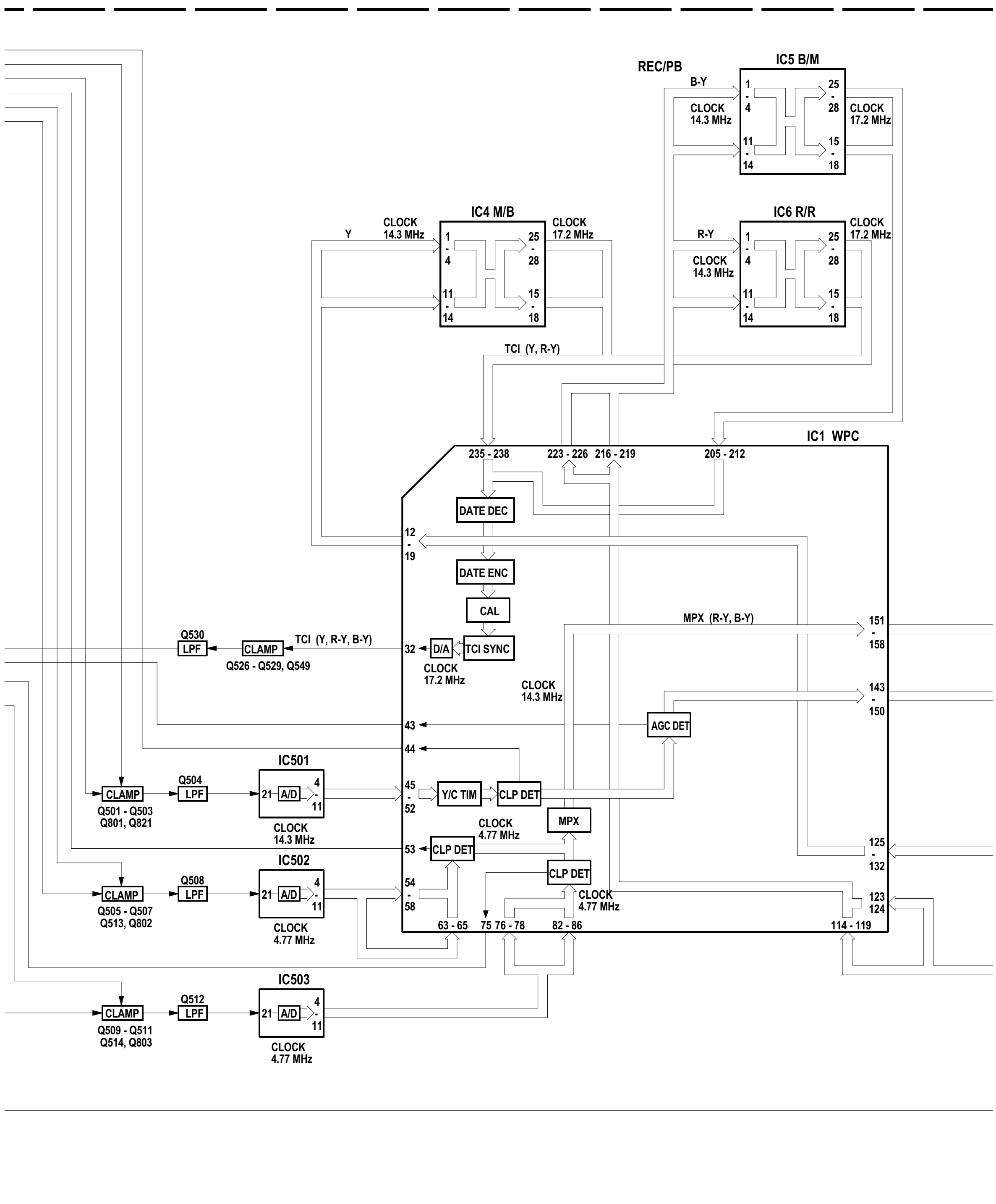


Fig. 3-2-4 Block Diagram of SD REC Mode Signal Processing (2/4)

• **SD REC mode signal processing (3/4)**

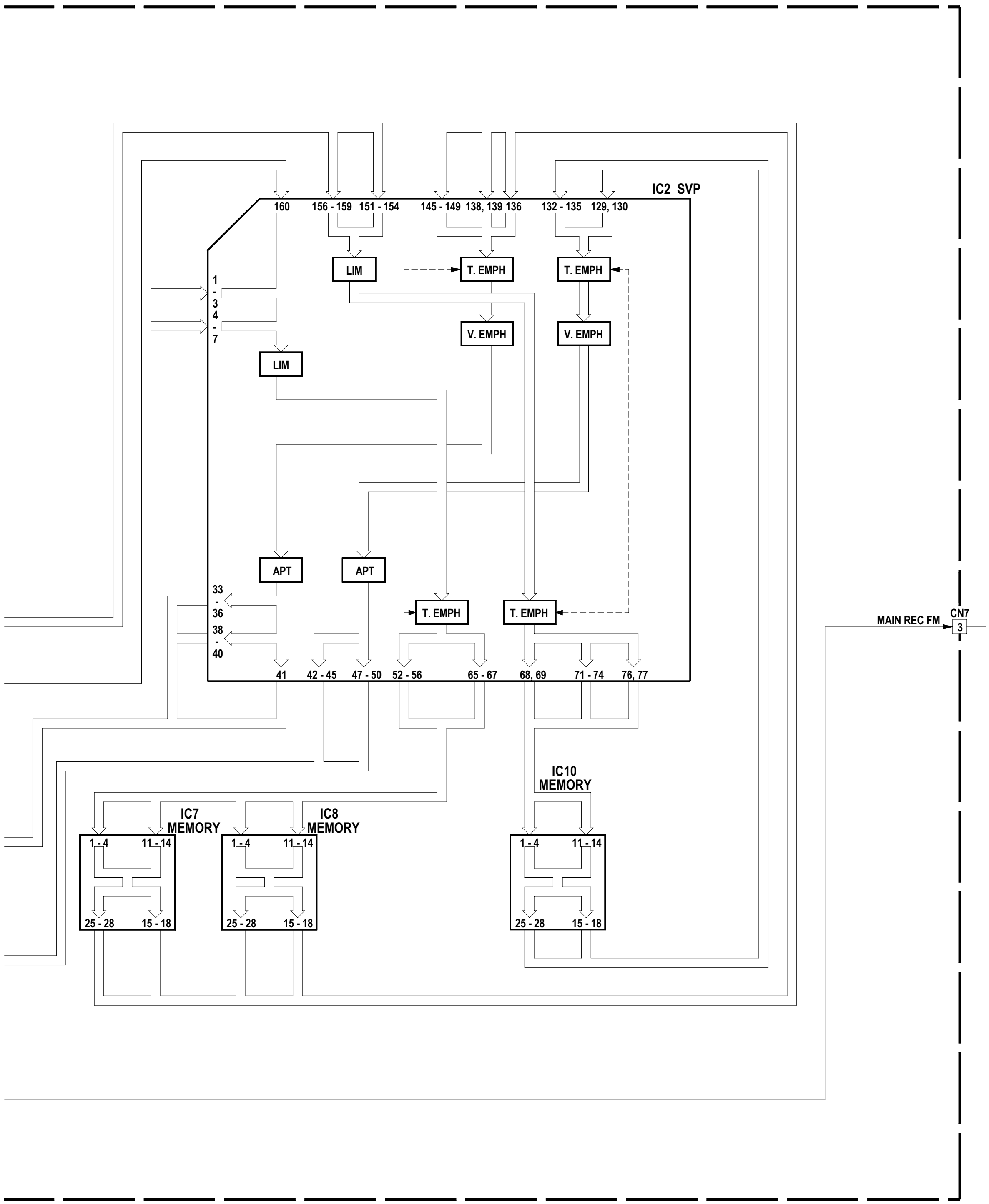


Fig. 3-2-4 Block Diagram of SD REC Mode Signal Processing (3/4)

• **SD REC mode signal processing (4/4)**

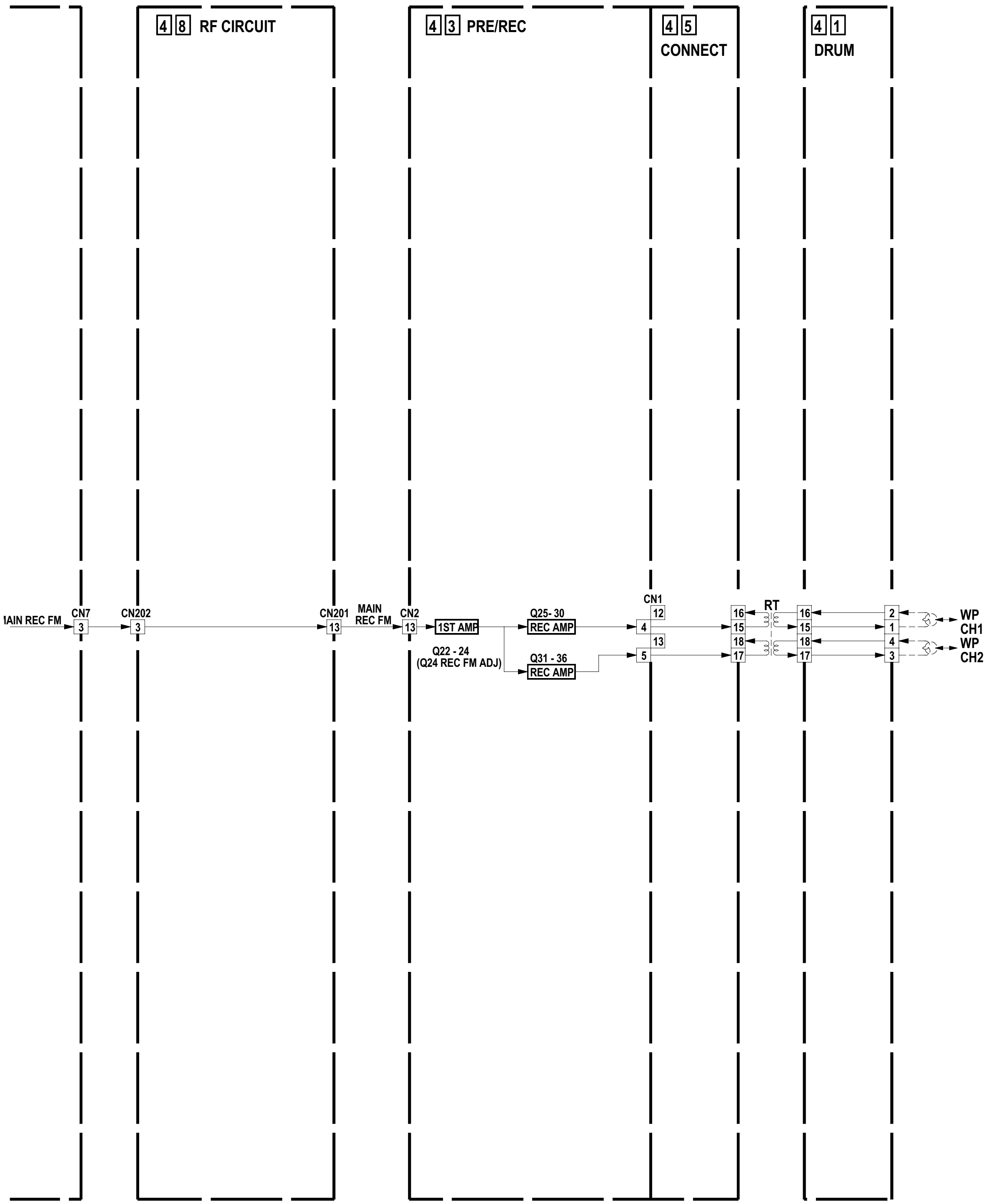


Fig. 3-2-4 Block Diagram of SD REC Mode Signal Processing (4/4)

3.2.5 SD PB MODE SIGNAL PROCESSING

In the signal processing of the SD PLAY mode, the process totally opposite to the signal processing of the SD REC mode is performed.

However the processes opposite to the chroma encoding and multiplexing in the signal processing of the SD REC mode are performed together by the 358C ENC 1/2 and 358C ENC 2/2.

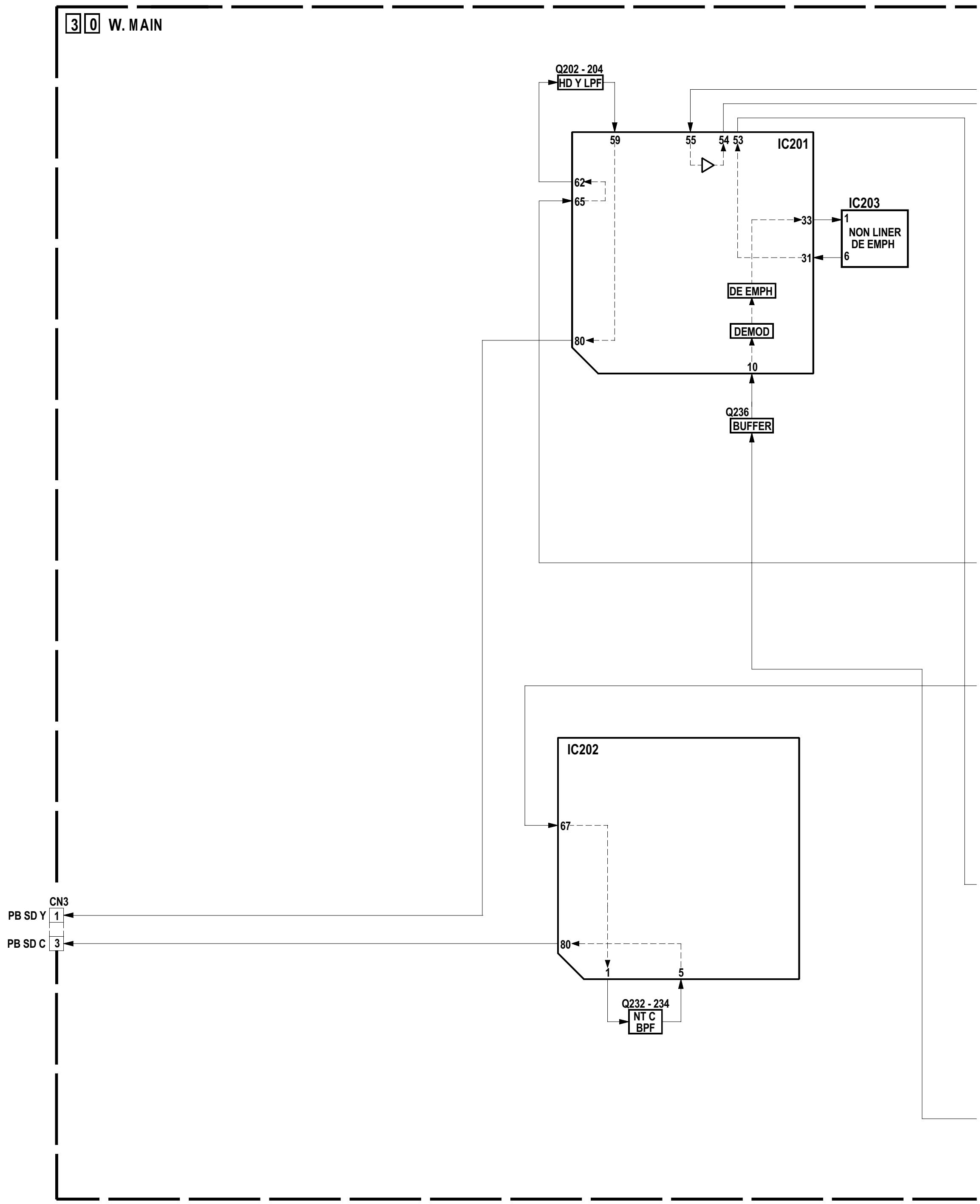


Fig. 3-2-5 Block Diagram of SD PB Mode Signal Processing (1/4)

• **HD PB mode signal processing (2/4)**

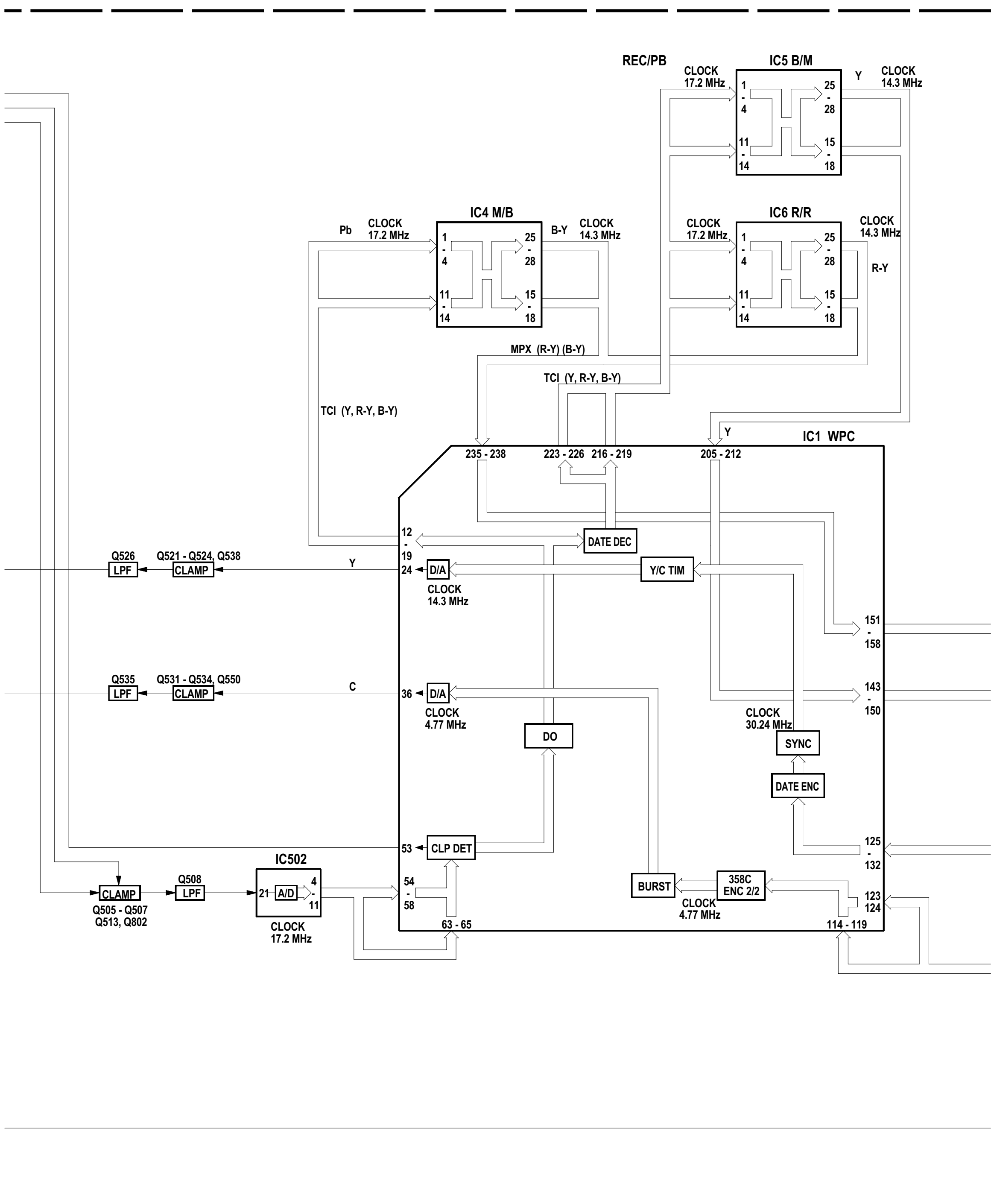


Fig. 3-2-5 Block Diagram of SD PB Mode Signal Processing (2/4)

• **HD PB mode signal processing (3/4)**

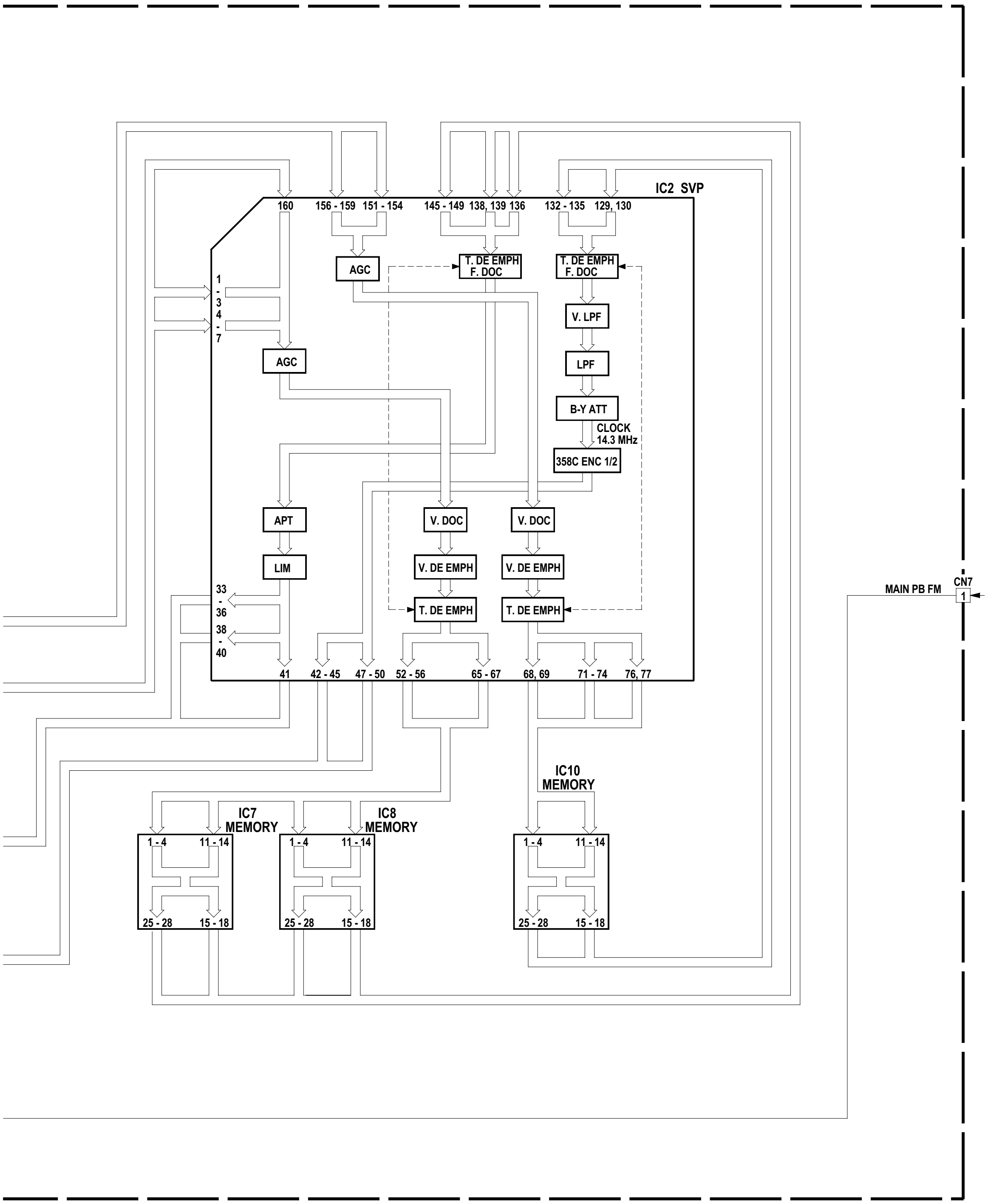


Fig. 3-2-5 Block Diagram of SD PB Mode Signal Processing (3/4)

• **HD PB mode signal processing (4/4)**

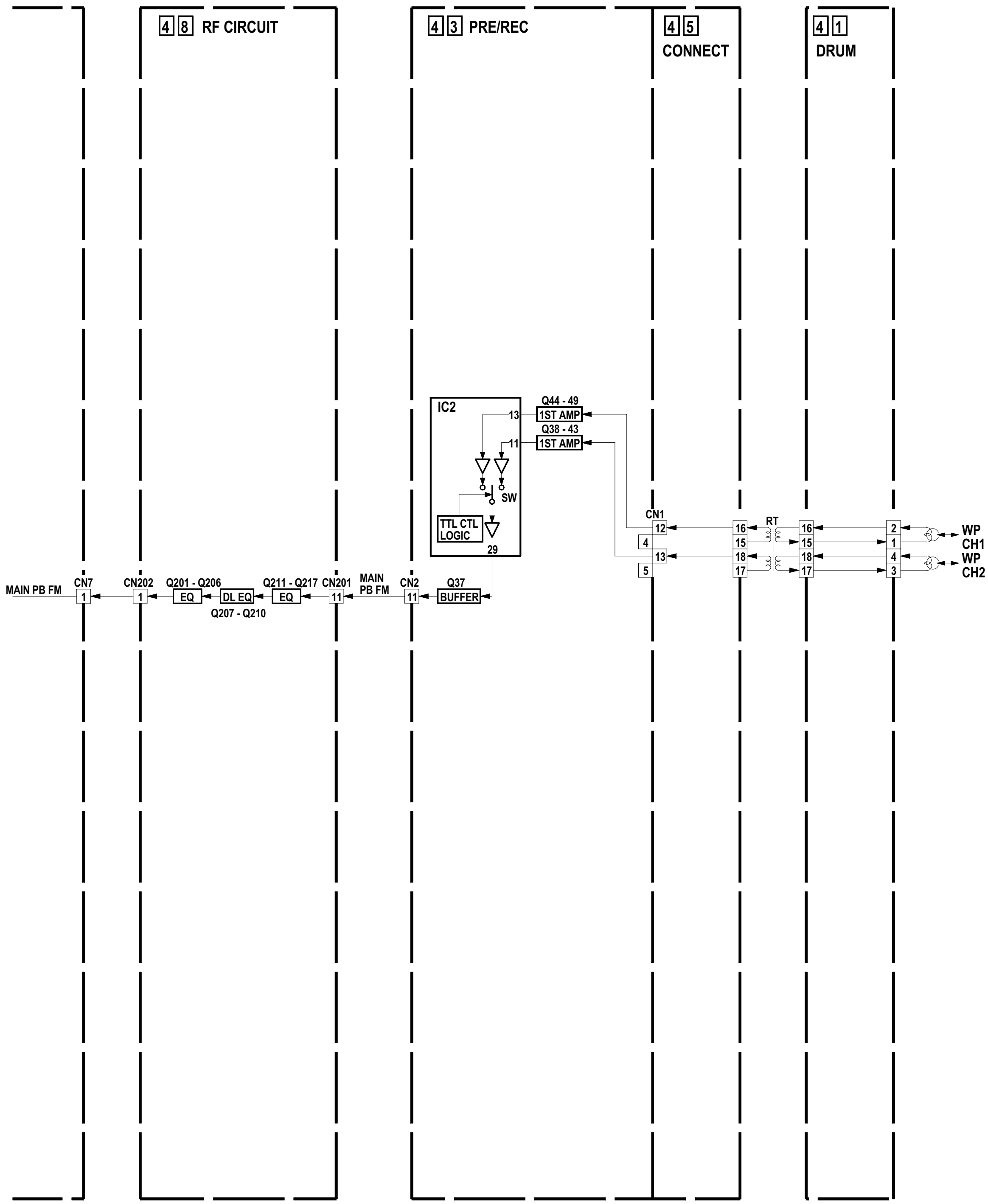


Fig. 3-2-5 Block Diagram of SD PB Mode Signal Processing (4/4)

3.3 W-VHS CLOCK SYSTEM

Fig. 3-3-1 shows the block diagram of the clock system of the W-VHS circuit of the SR-W5U.

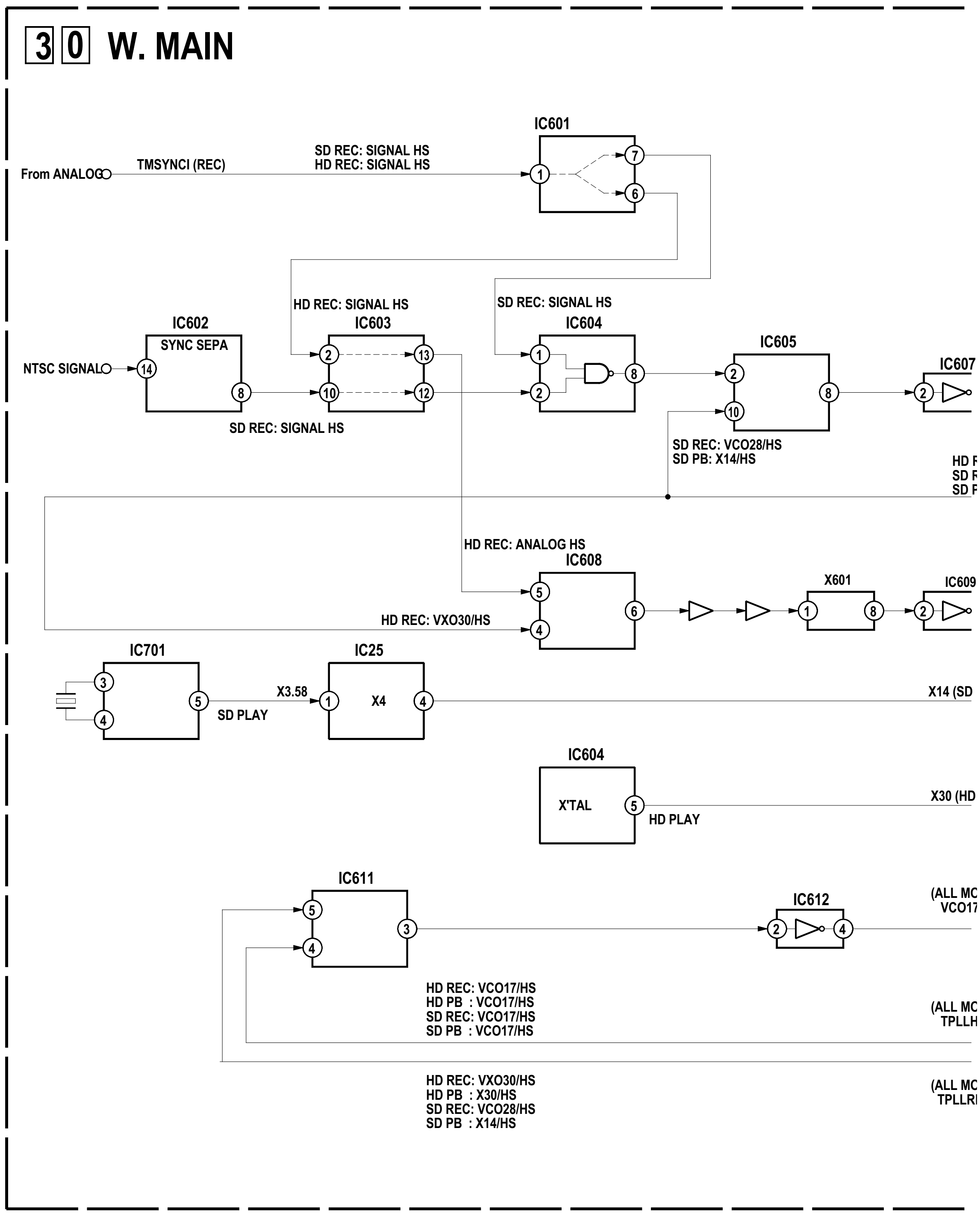


Fig. 3-3-1 Block Diagram of SR-W5U Clock System (1/2)

• **W-VHS clock system (2/2)**

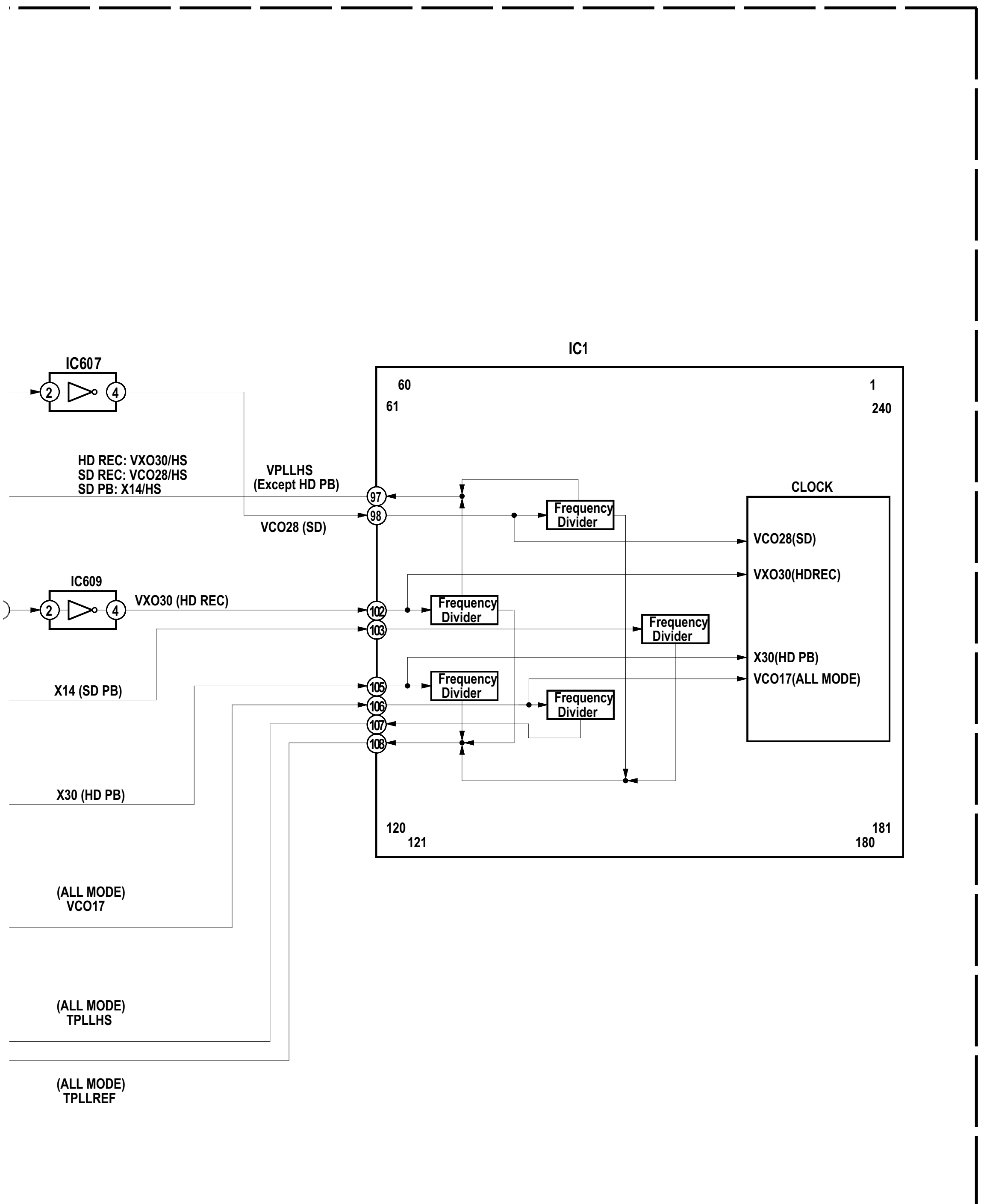


Fig. 3-3-1 Block Diagram of SR-W5U Clock System (2/2)

3.3.1 HD REC mode clock system

In the HD REC mode, VXO30 (generated in the PLL circuit from the H sync made by frequency-dividing itself and H sync from input signals) serves as the reference of the other clocks.
Each clock is generated by inputting the H sync generated by frequency-dividing VXO30 and the H sync made by frequency-dividing itself in the PLL circuit.

3.3.2 HD PLAY mode clock system

In the HD PLAY mode, X30 (IC6 X'TAL) serves as the reference of the other clocks.
Each clock is generated by inputting the H sync generated by frequency-dividing this X30 and the H sync made by frequency-dividing itself in the PLL circuit.

3.3.3 SD REC mode clock system

In the SD REC mode, VCO28 (generated in the PLL circuit from the H sync made by frequency-dividing itself and H sync from input signals) serves as the reference of the other clocks.
Each clock is generated by inputting the H sync generated by frequency-dividing VCO28 and the H sync made by frequency-dividing itself in the PLL circuit.

3.3.4 SD PLAY Mode Clock System

In the SD PLAY mode, X14 (IC701 X'TAL 358 is multiplied four times in IC25) serves as the reference of the other clocks.
Each clock is generated by inputting the H sync generated by frequency-dividing this X30 and the H sync made by frequency-dividing itself in the PLL circuit.

3.4 W-VHS SPECIAL PLAYBACK SYSTEM

Fig. 3-4-1 shows the flow of signals during special playback of the SR-W5U.

In the W-VHS, playback signals are subject to sampling at 8 bits, but during special playback, the envelope detection signal of the color signal is input as data to the LSB of the color signal. Based on the value of this envelope detection signal, the method of compensating signals during special playback is switched by frame memory processing.
General video signals are transferred by 8 bits, but transfer of color signal by 7-bit output presents no visual problems.
The luminance signals are used as they are. As there are no envelope detection signals for luminance signals, the compensation method of signals is switched based on the envelope detection signals of color signals of the same line.
By using this system, signals during the search and slow modes can be compensated without the need to use memories other than that for normal playback.
The time differences in the delay of envelope detection signals and playback signals match and signal compensation is accurate in this model. Because the capacity of the TCI conversion memory is made 1 field and memory reset is performed every 1 field, this has reduced the number of outpacing which occurs between writing and reading of the memory and decreased uncontinuous portions in signals after TCI conversion.

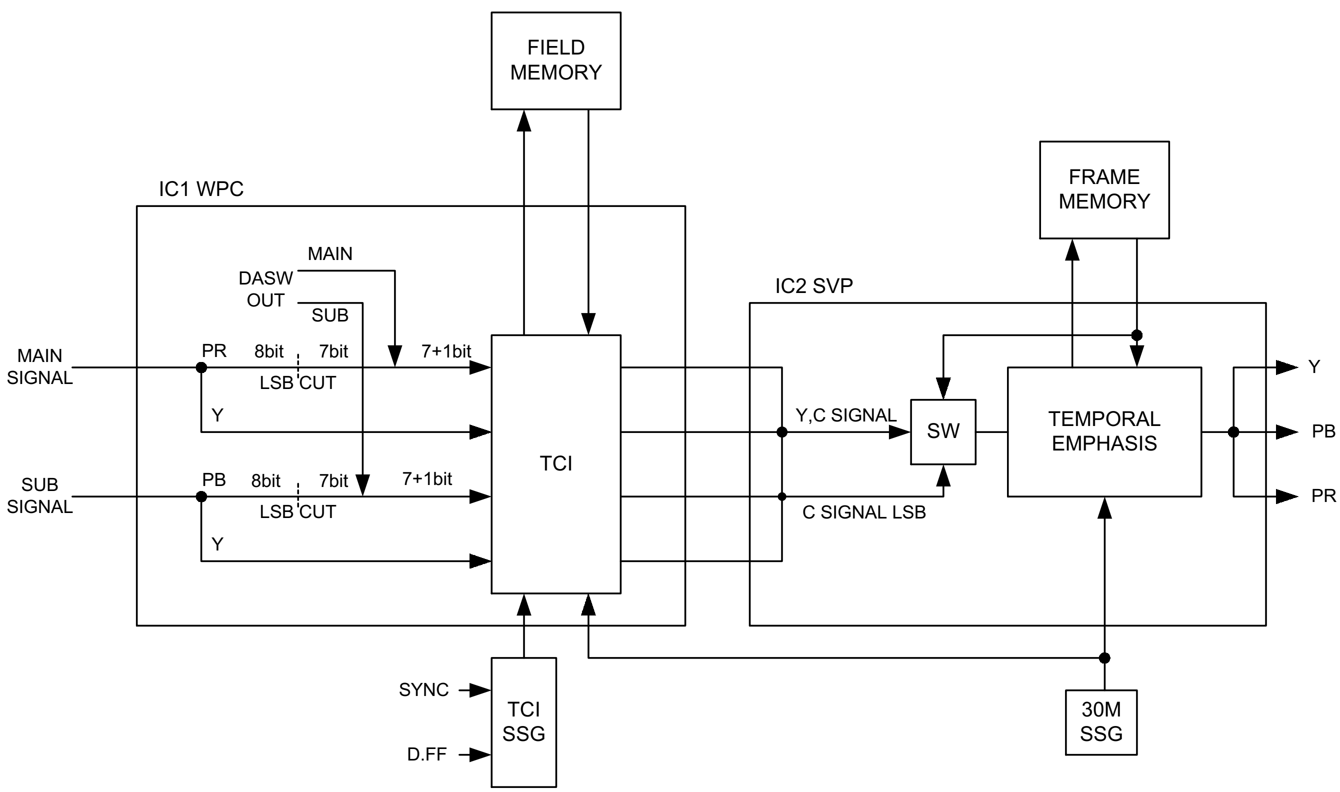


Fig. 3-4-1 Signal Processing during Special Playback

3.4.1 Operations during search

By setting the counter values of the rising and falling of the D.FF, the SSG V counter used for TCI processing synchronizes writing of the field memory with the D.FF. At this time, the FF.TBC does not operate but the temporal deemphasis does.
The presence of Main and Sub signals is differentiated using the DAWS in IC1 (WPC) from envelope signals. Fig. 3-4-2 shows the timings of the generation of the DASW envelope detection signals.
Based on this detection signal, the TCI signal is made 00 when the envelope signal is absent from both heads, the LSB of the color signal of the TCI signal is made 1 for the self head signal, and the LSB of the color signal of the TCI signal is made “0” for the reverse head signal.
After this, the TCI signal is sent to the SVP via the field memory.
When the signals of both heads are present at the SVP, both heads compensate their own signals. When signals are present at only one head, the signals of the other head are compensated by the signals of one head, and when signals are absent from both heads, the signals of the heads are compensated by the previous frame signals by the frame memory output. This frame memory complete images field by field in field operations. At this time, the temporal deemphasis operates. As the drum servo is locked so that the fH becomes a positive value, the rotation speed of fV deviates.

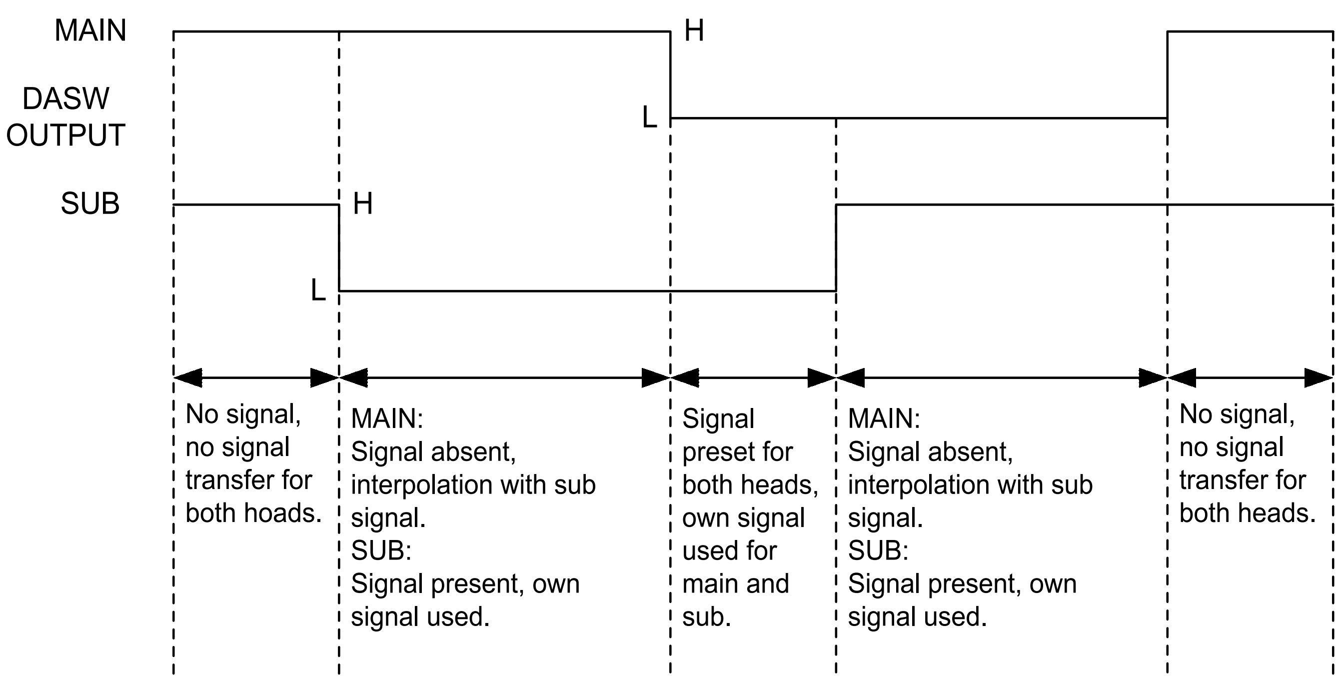


Fig. 3-4-2 DASW envelope detection signals timing chart

3.4.2 Operations of normal direction slow mode

The slow mode of the SR-W5U is an intermittent slow mode and
differs from the mechanical operations of the intermittent slow mode of normal VHS. The following describes the ×1/6 speed slow mode as an example.

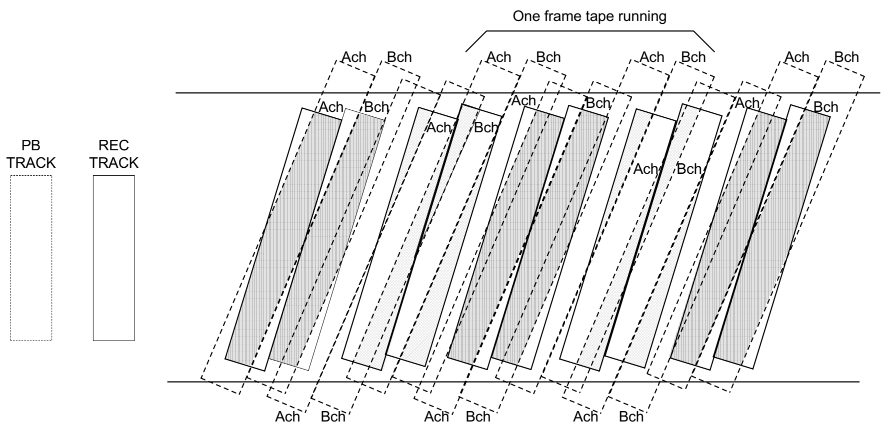


Fig. 3-4-3 Head Trace Pattern during ×2/3 Speed Running

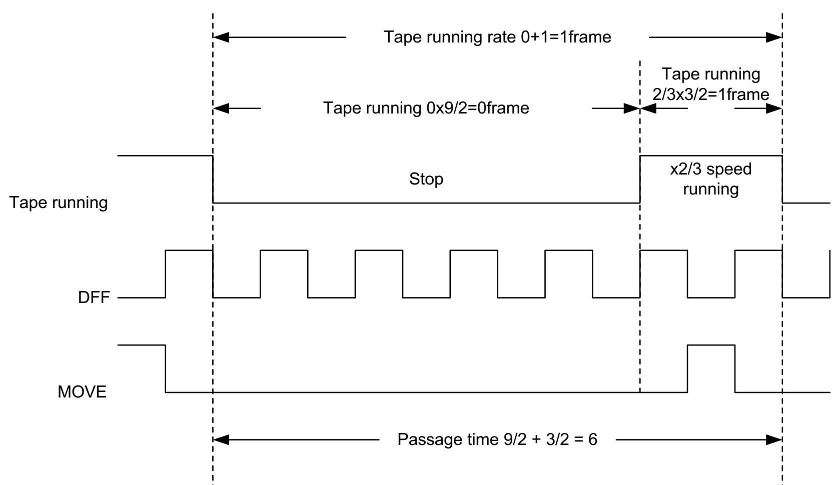


Fig. 3-4-4 Timing Chart during ×1/6 Speed Slow Mode

As shown in Fig. 3-4-3, when the 3/2 frame is traced by ×2/3 speed running, the tape is forwarded by one frame of normal playback, and at this time, the envelope signal of one field can be extracted. The signals at this time are used as images. After this, tape running is stopped during 9/2 frames.
×1/6 speed slow is performed by repeating these two operations.
This is because, as shown in Fig. 3-4-4, these two operations require a time of 12/2 frames, which is 6 frames, and during this time, the tape has only forwarded by one frame.
The normal rotation slow modes of other speeds also trace 3/2 frames at ×2/3 speed running, the tape is forwarded by one frame of normal playback, and the same operations are performed until an envelope signal of one field is extracted. After this, the length of the time for stopping tape running is changed to change the speed of the slow mode.
Actually, at first, it was planned that one frame be traced at ×1 speed running, and after extracting a 1 frame complete envelope, tape running be stopped at the appropriate period, and slow modes of various speeds be performed. However, as the SR-W5U did not have a function to stabilize this operation, operations have been changed as described above.
During normal direction slow, the W-VHS circuit operates as follows.
Only when the period (MOVE:H) where playback signals of both heads are present at the WPC DASW and the capstan is operating, the LSB of the color signal is set to “H”, and sent to the SVP.
In the SVP, playback signals are used during the above periods. In other periods, frame memory signals are output, compensation is carried out using the signals of the previous frame. Like in the search mode, the frame memory performs field operations, and compensate images field by field. At this time, temporal deemphasis operations are carried out.

3.4.3 Operations of Reverse Slow Mode

The basic concept is the same as the normal direction slow mode. The following describes operations taking ×1/3 speed slow as an example.

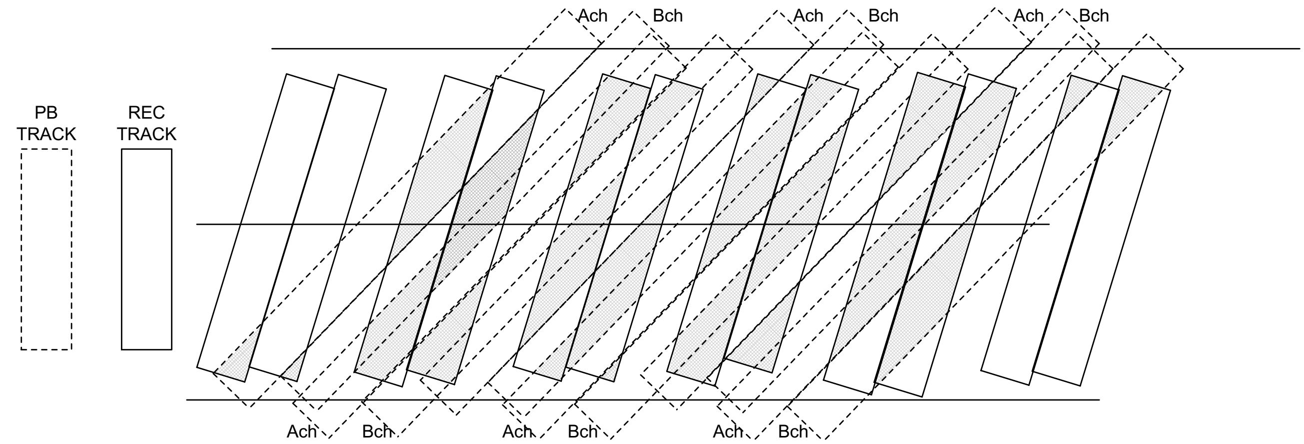


Fig. 3-4-5 Head Trace Pattern during ×–2/3 Speed Running

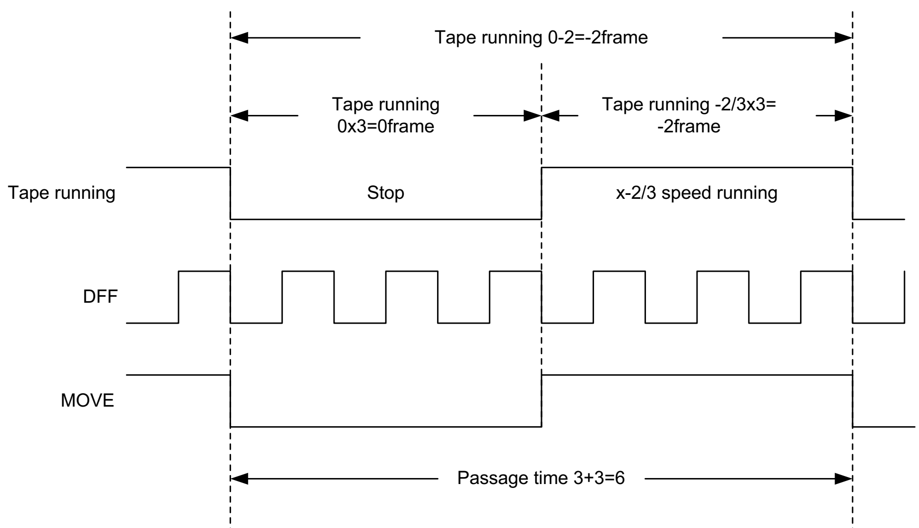


Fig. 3-4-6 Timing Chart during ×1/6 Speed Slow

As shown in Fig. 3-4-5, when three frames are traced by ×–2/3 speed running, the tape forwards for two frames of normal playback. The difference from normal direction slow is the envelope is divided over extending over tracks. But as images are completed by performing compensation in the W-VHS circuit, this reverse slow mode is satisfactory. After this, tape running is stopped during a period of three frames.
×1/3 speed slow is performed by repeating these two operations.
This is because as shown in Fig. 3-4-6, these two operations require a time of 12/2 frames, which is six frames, and during this time, the tape only forwards for two frames.
The reverse slow modes of other speeds also trace three frames by ×–2/3 speed running, and the tape is forwarded by two frames of normal playback. After this, the length of the time for stopping tape running is changed to change the speed of the reverse slow mode.
The W-VHS circuit operates in the same way as during the normal direction slow mode.

3.3.4 Still operations

Only the writing of the frame memory is stopped.

3.4.4 DASW (Color Signal Envelope Detection Signal Generation Circuit) Operations

Fig. 3-4-7 shows the timing diagram of the DASW envelope detection signal detection.

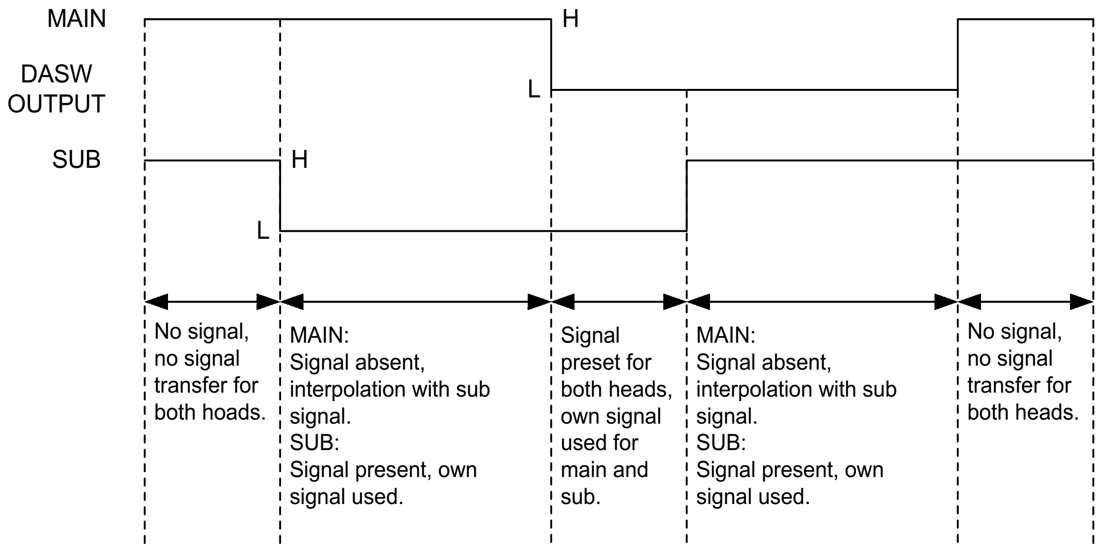


Fig. 3-4-7 DASW envelope detection signals timing chart

Whether the head output signal is sent from the self head or the reverse head is determined according to the respective envelope signals.

When the respective envelope signals for the Main and Sub signals are present, the L detection signal is output. When absent, the H detection signal is output.

Based on this detection signal, the TCI signal is made 00 when the envelope signal is absent from both heads, the LSB of the color signal of the TCI signal is made 1 for the self head signal, and the LSB of the color signal of the TCI signal is made “0” for the reverse head signal.

SECTION 4
3D VSP/TBC CIRCUIT

4.1 PRINCIPLE OF 3D VSP/TBC CIRCUIT

The 3D VSP/TBC circuit performs YC separation of the composite video signals mainly during EE/recording and processings such as TBC and various noise reductions during playback.

4.1.1 Signal processing during EE/REC (Y/C separation)

Fig. 4-1-1 shows a block diagram of the signal processing during the EE/recording mode.

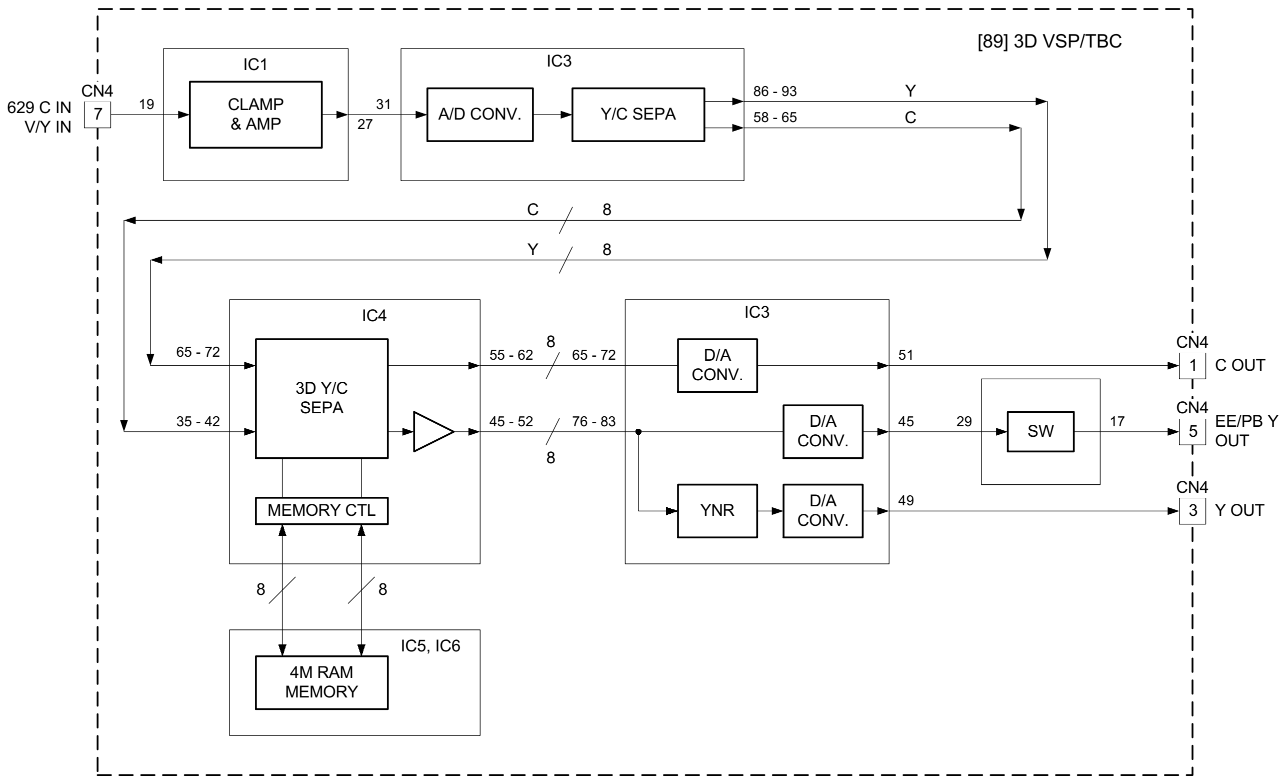


Fig. 4-1-1 Block Diagram of Signal Processing during the EE/Recording Mode

4.1.2 Flow of signals during PB mode

Fig. 4-1-2 shows the principle of PB signal flow of the 3D VSP/TBC circuit block diagram.

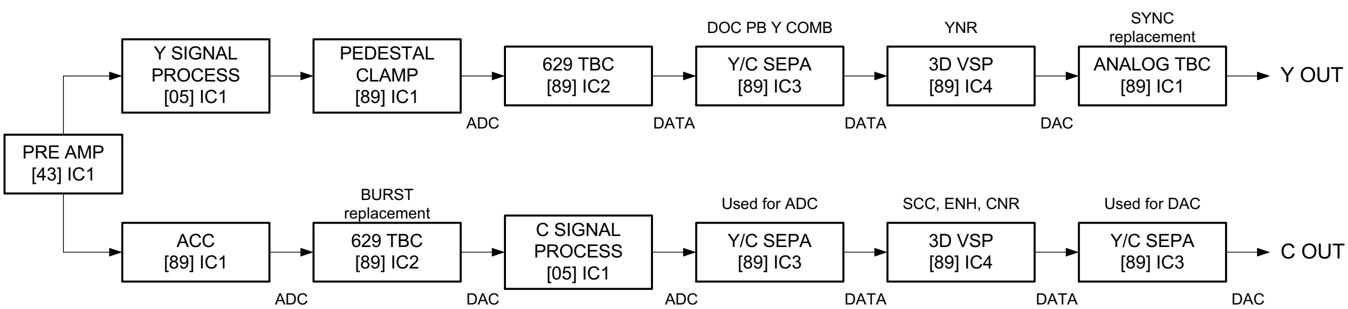


Fig. 4-1-2 Principle of 3D VSP/TBC ciruit block diagram.

Fig. 4-1-3 shows the block diagram of signal processing during the PB mode.

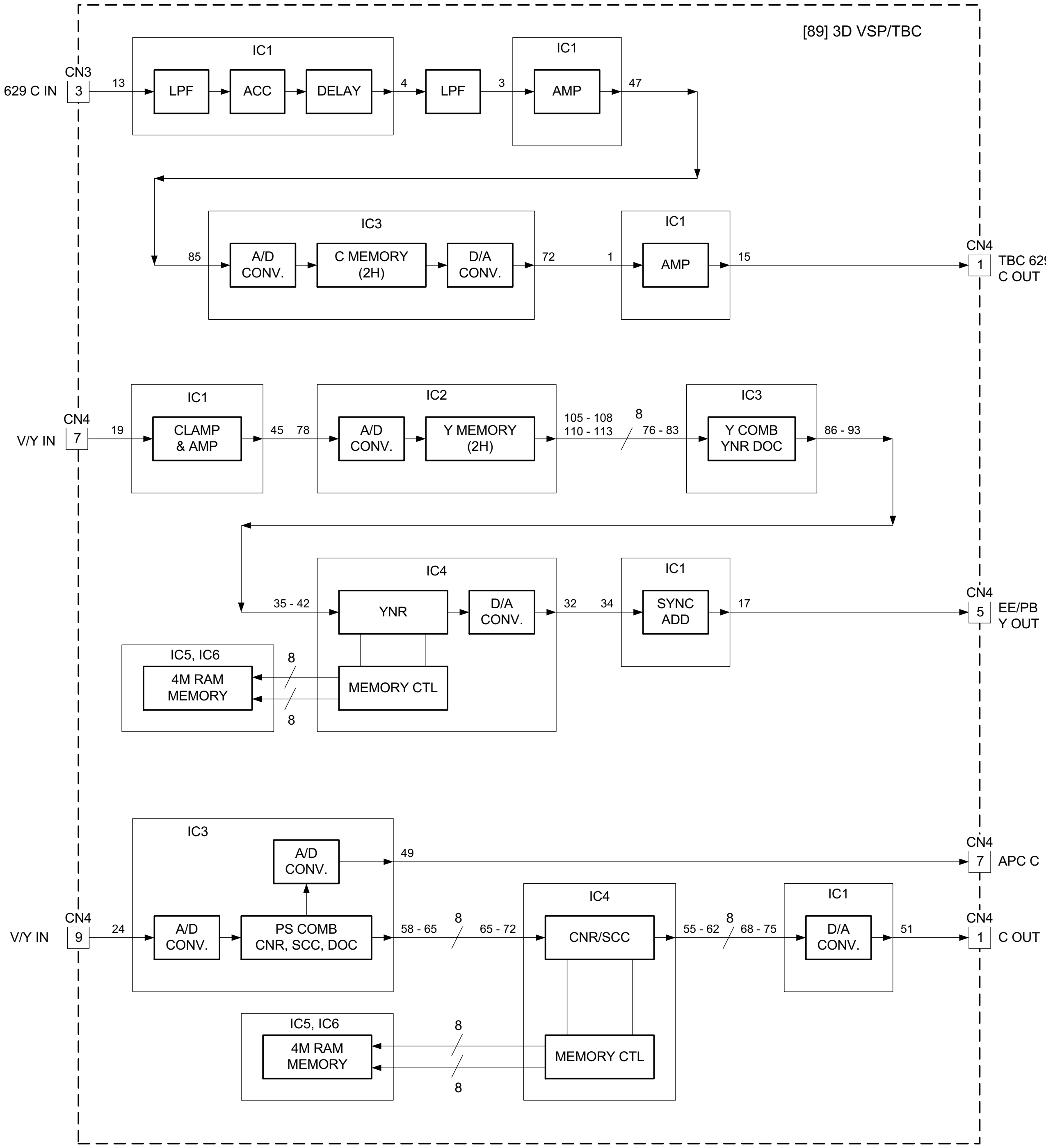


Fig. 4-1-3 Flow of Signals During PB Mode

4.2 New Technologies for the 3D VSP/TBC Circuit

4.2.1 3D super color system

Various methods for resolving “color blurring” and “missing colors” during playback which occur due to the restriction of the bands of the color signals are being developed for the VHS and S-VHS.

With the conventional methods, basically, there also exists a strong correlation between the color signals, and compensation is carried out using the edge information of broad band luminance signals. However, with these methods, sufficient effects cannot be obtained for pictures that lack correlation in which the luminance does not change and only the colors change considerably.

In this system, to resolve these problems, the band of the color signal is improved using the past edge of the color signal itself.

Fig. 4-2-1 shows the block diagram of the 3D super color system.

Signals of one frame before compensated in the correlation processing block are input to the current frame and correlation processing block, and signals which join only correlating portions are output.

After this, only the high band components which are required for compensation are passed through the HPF, added to the current frame signal, and output.

At the same time, this signal is delayed by one frame by the frame memory, and used for the next frame compensation. Hereafter, this process is repeated to enhance only the high band components of portions with frame correlation. As a result, more minute compensation with little noise components can be performed.

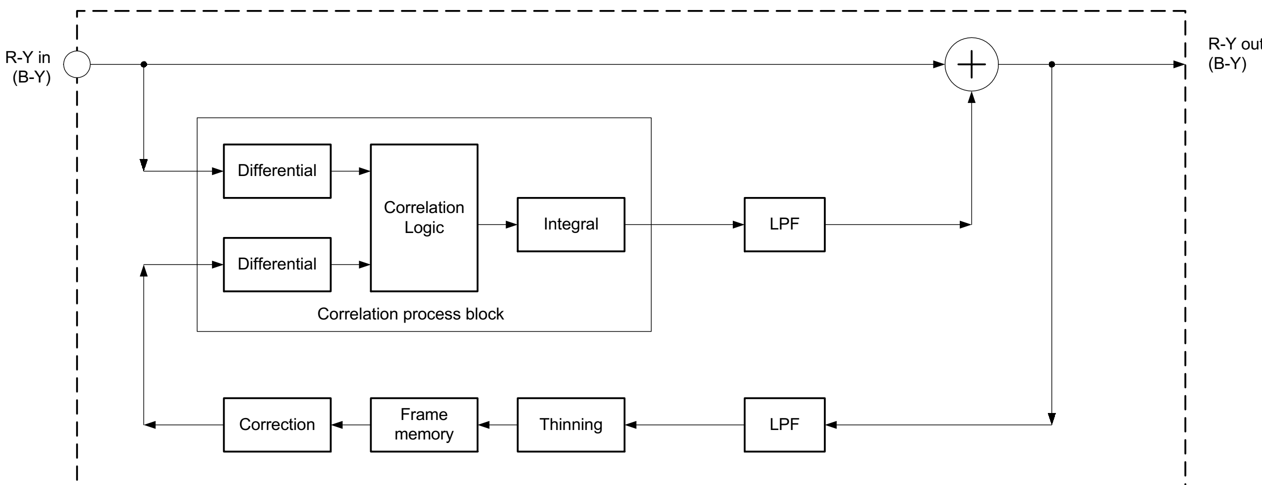


Fig. 4-2-1 Block Diagram of 3D Super Color System

4.2.2 New 629 digital TBC

The TBC (Time Base Collector) is a system which eliminates screen distortions and reproduces stable images by compensating time axis deviation (jitter) of scanning lines which occurs due to the tape running system.
This unit mounts a 629 digital TBC. As the 629 digital TBC performs time axis compensation of the color signal (629 kHz) and luminance signal which have been converted to low bands, changes in hue which occur secondarily due to jitters are decreased. Compared to the conventional TBC, it demonstrates higher effects for high band jitters.
Fig. 4-2-2 shows the block diagram of the basic configuration of the TBC circuit.

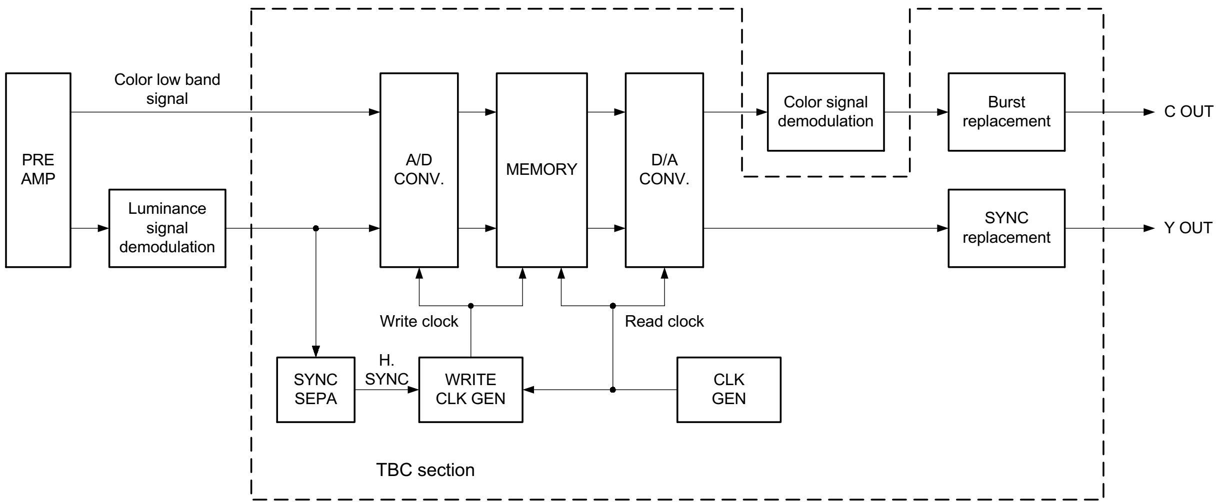


Fig. 4-2-2 Block Diagram of Basic Configuration of TBC Circuit

The write clocks generated from the WRITE CLK GEN is 4 fsc frequency synchronized with the H. SYNC of the input signals, and therefore, 1H signals are also sampled for 910 times by this clock. As a result, the luminance signal are eliminated of the jitter components in the stage where they are written in the memory. Reading from the memory is performed by the clock generated by X'TAL using the logical 4 fsc of the NTSC, and therefore jitter-free luminance signals can be obtained.

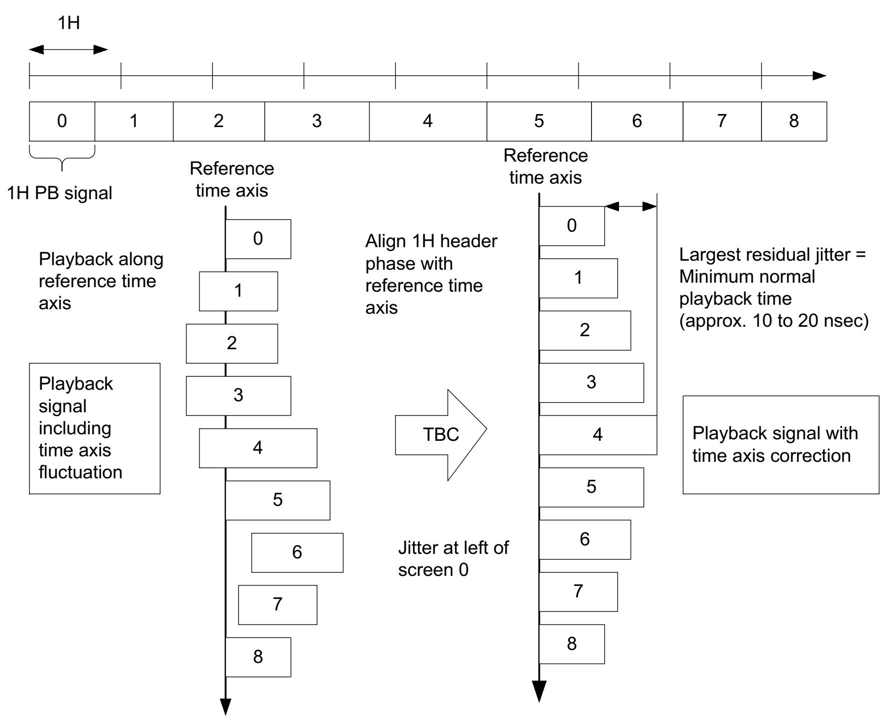


Fig. 4-2-3 Compensation of Jitters of TBC Circuit

As shown in Fig. 4-2-3, this system eliminates jitters by resetting the write address in the line memory when writing the playback signal in the memory at the SYNC timing, and matches the head of the horizontal period to that of the line memory and writes.
As for the method of generating the write clock, the AFC method using VCOs like PLL are not used. Instead an APC method which enables clocks to be obtained immediately according to the jitter by supplying fixed clocks oscillation by a stable X'tal to the multi-stage delay element, generating many clocks with slightly different phases, and selecting the phase clock nearest to the SYNC signal from among.
Fig. 4-2-4 shows the write clock generation circuit and its operations.

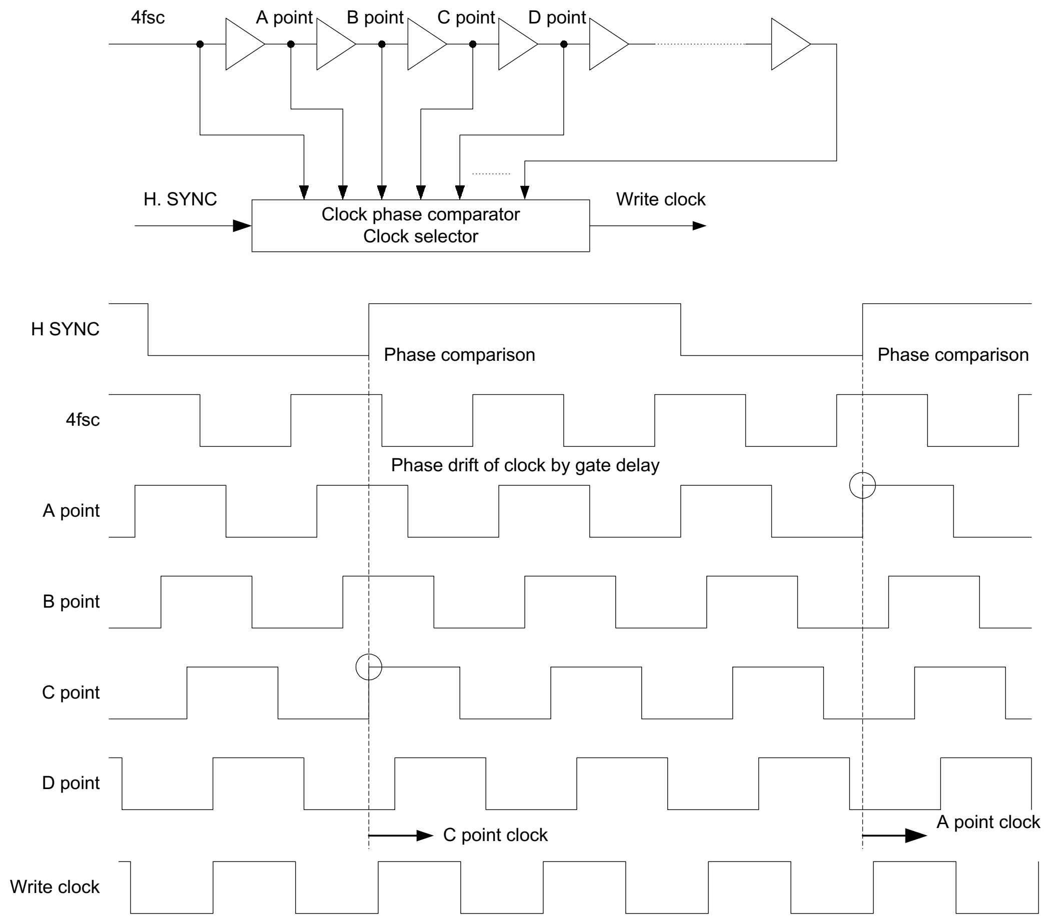


Fig. 4-2-4 Write Clock Generation Circuit and Its Operations

As this method does not have a field forward configuration without a feedback loop like the PLL, the jitters of every line can be compensated without any delay in phase. Consequently, the use of this method has enabled the realization of a system with high speed response corresponding to switching points such as head impact errors and skew during search. The line APC method compensates the jitters of each line completely, but not the velocity error, which is the time axis deviation components within one line. Therefore remainder jitters are greatest at the end of one line or at the right edge of the screen.

When the horizontal sync frequency is taken as fH, the degree of remainder jitters E(F) below fH/2 is $E(f)=2\sin\pi(f/fH)$. Fig. 4-2-5 shows this characteristic.

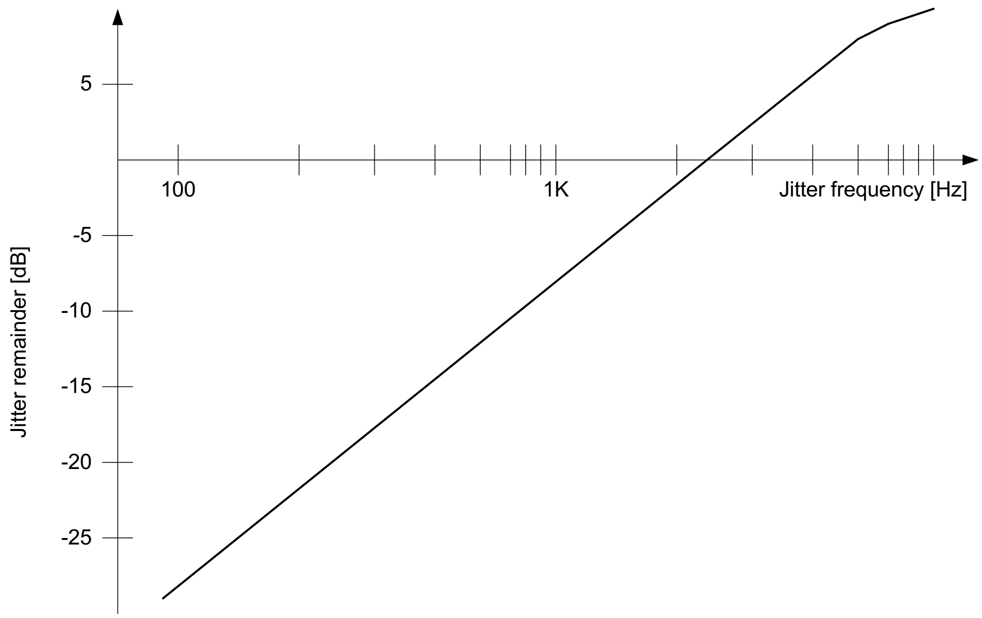


Fig. 4-2-5 Jitter Remainder Characteristics

Refer to Fig. 4-2-2. In this system, using the advantages of the built-in type TBC in the VCR, the TBC is placed in front and at the back of the color signal demodulation system and time axis compensation is performed in the low band color signal stage to realize elimination of phase deviation caused by jitters. This method offers the merit of having no image deterioration caused by encoding and decoding which could not be avoided in the conventional TBC processing color signals using color difference signals.

SECTION 5
VIDEO CIRCUIT

5.1 VIDEO CIRCUIT SIGNAL FLOW
5.1.1 Signal flow at REC mode

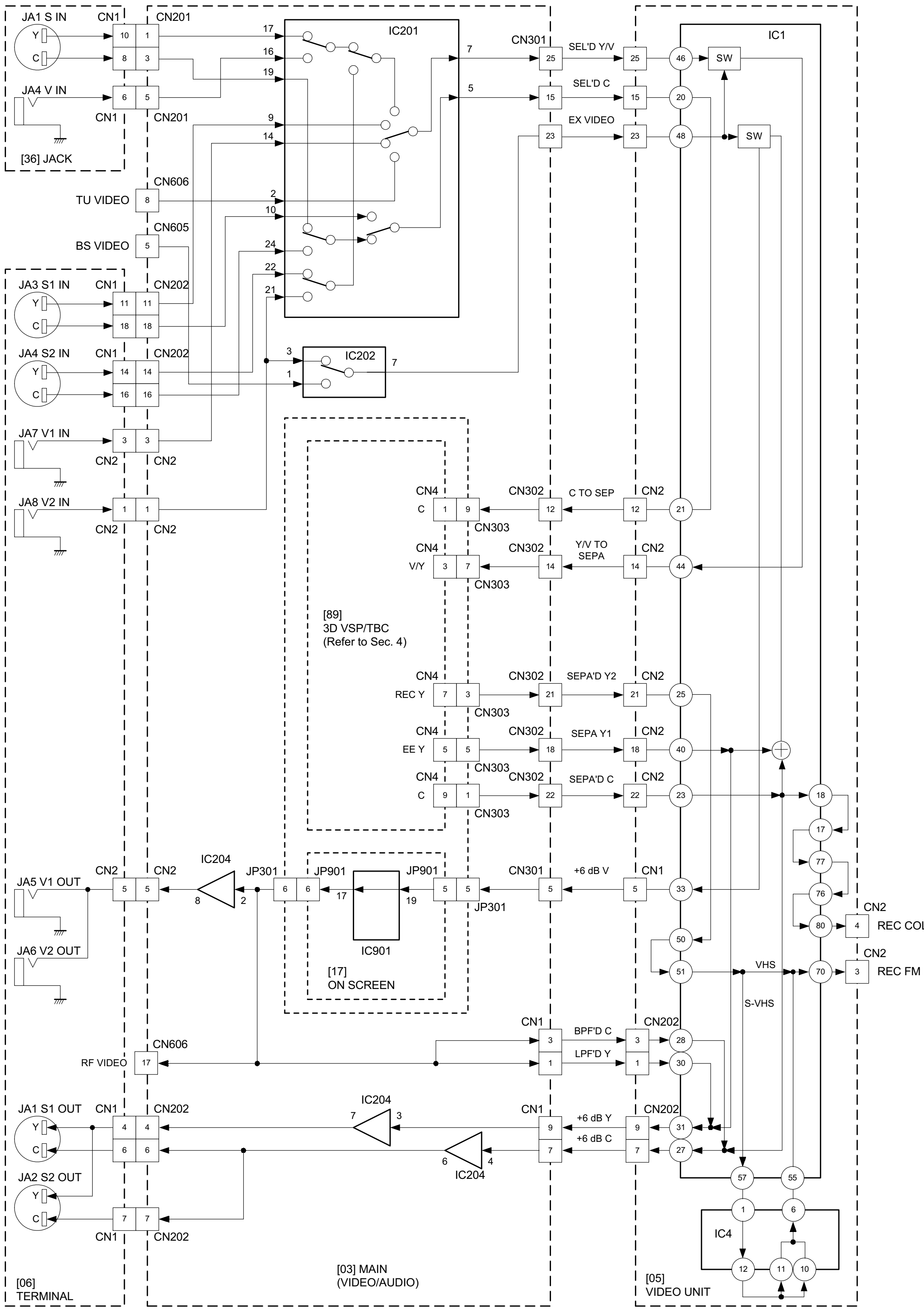


Fig. 5-1-1 Signal flow block diagram at REC mode

5.1.2 Signal flow at EE mode

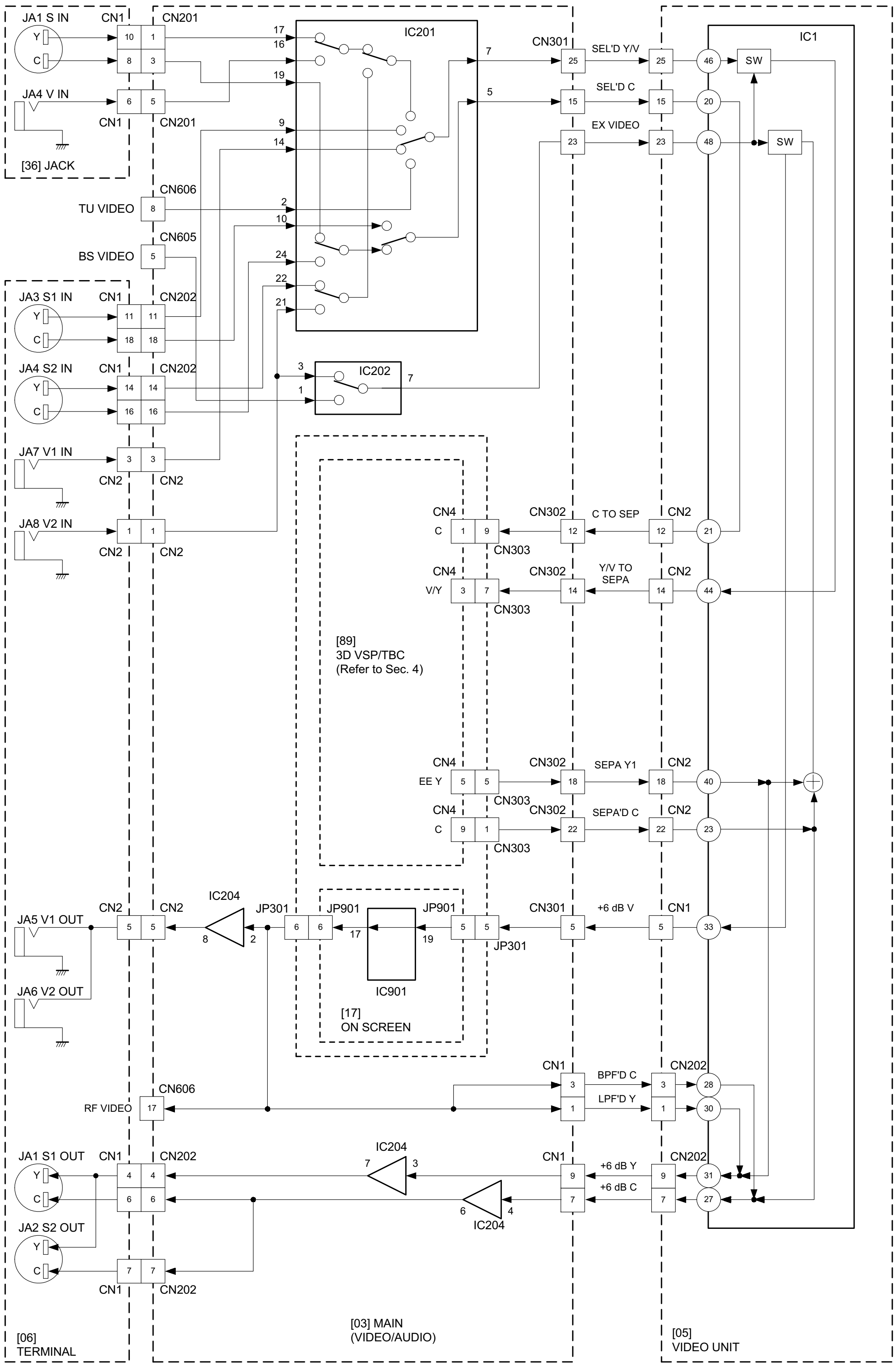


Fig. 5-1-2 Signal flow block diagram at EE mode

5.1.3 Signal flow at PB mode

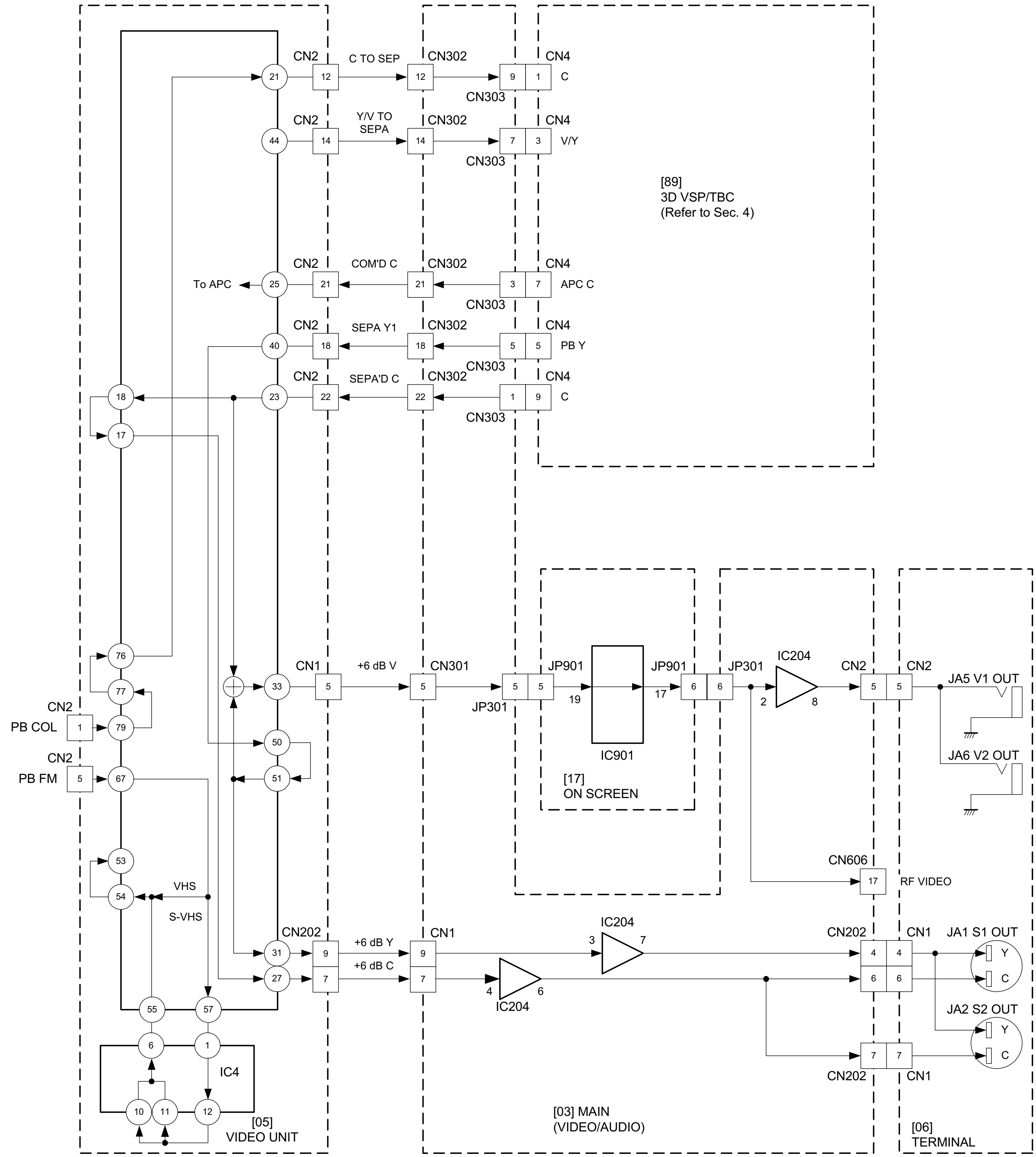


Fig. 5-1-3 Siganl flow block diagram at PB mode

SECTION 6
AUDIO CIRCUIT

6.1 AI HYPER TANGENT

The tilt of the audio signal changes greatly from positive to negative near the peak as shown at (a) in Fig. 6-1-1, and does not change more or less near the zero cross point at (b) in the figure. On the contrary the absolute value of the signal does not change more or less near the peak, but changes considerably near the zero cross point. Focusing on this point, if there exists a zero cross point as (b) between the overlapped portion of the FM signals of two heads, the AI hyper tangent method performs switching at this zero cross point, and compensation of the tilt by differential is performed for the distortion of the waveform.
If there is no zero cross point as (b) at the overlapped portion, it performs compensation during switching by peak hold as shown at (a). As shown in Fig. XX, with this method, the compensation error is relatively small, but the end point of compensation does not join the signal waveform continuously. Consequently, this portion is further compensated by using the additional pulse.

6.1.1 Zero cross switching circuit

Fig. 6-1-2 shows the block diagram of the zero cross switching circuit which controls the switching of the compensation method.

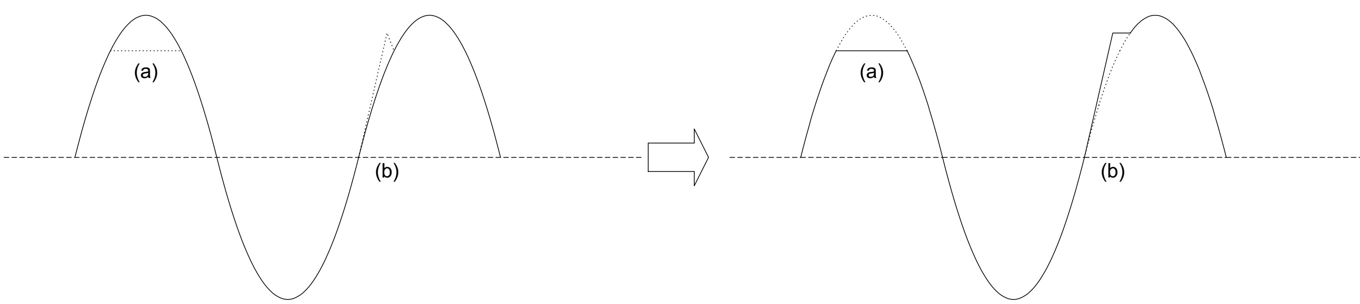


Fig. 6-1-1 Audio Signal Waveform

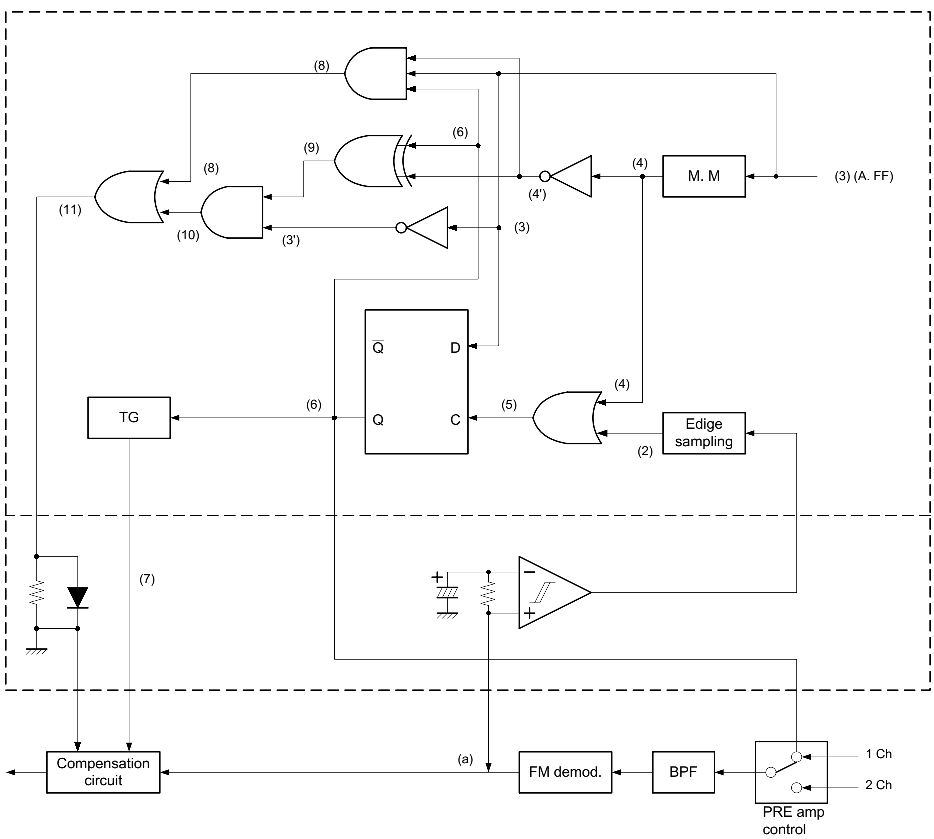


Fig. 6-1-2 Block Diagram of Zero Cross Switching Circuit

6.1.2 Zero cross switching circuit operations

The demodulated audio signal (a) is input to the comparator to obtain (1) shown in Fig. 6-1-3. This is supplied to the edge extraction circuit, to obtain a signal (2) which is a pulse corresponding to the zero cross.
Next, AFF (3) is input to the mono-multi circuit (M.M) to obtain the signal (4) which becomes “L” during 130 µs from the switching of (3). Then the OR of (2) and (4) is obtained to obtain (5) at which the zero cross point during the time when (4) becomes “L” is detected. Taking this (5) as the clock and (3) as the data, they are input to the D Type Flip
Flop, and the output (6) is input to TG (timing generator) to create an approximately 15 µs compensation pulse (7).
The approximately 130 µs period set for signal (4) was set so that zero cross switching is performed during the overlapping of the FM signals accurately, taking into consideration inaccuracy of the adjustment of the switching pulse for switching the preamplifier (standard:2H:127 µs).

If there is no zero cross point while (4) is “L”, the D Type Flip Flop output (6) is inverted when (4) is switched. Next, the AND of (6), (3), and (4') shown in Fig. 6-1-4 is obtained, and the pulse (8) becomes “H” only when there is zero cross point when (3) is “H”.
Next, when (3) is “L”, (9) is made by obtaining the EX-OR of (6) and (4'), and then the AND of this (9) and (3') is obtained to obtain the pulse (10) which becomes “H” if the zero cross point exists. The OR of the pulses (8) and (10) is then obtained here to generate the pulse (11) which becomes “H” if the zero cross point exists during the overlapping period. This becomes the signal which controls the compensation method.

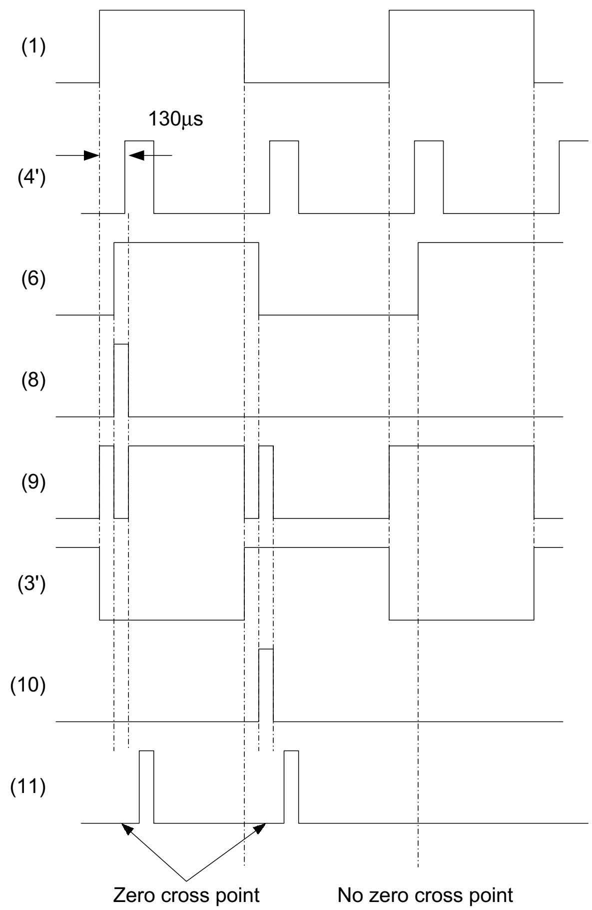


Fig. 6-1-4. Zero Cross Switching Circuit Internal Waveform-2

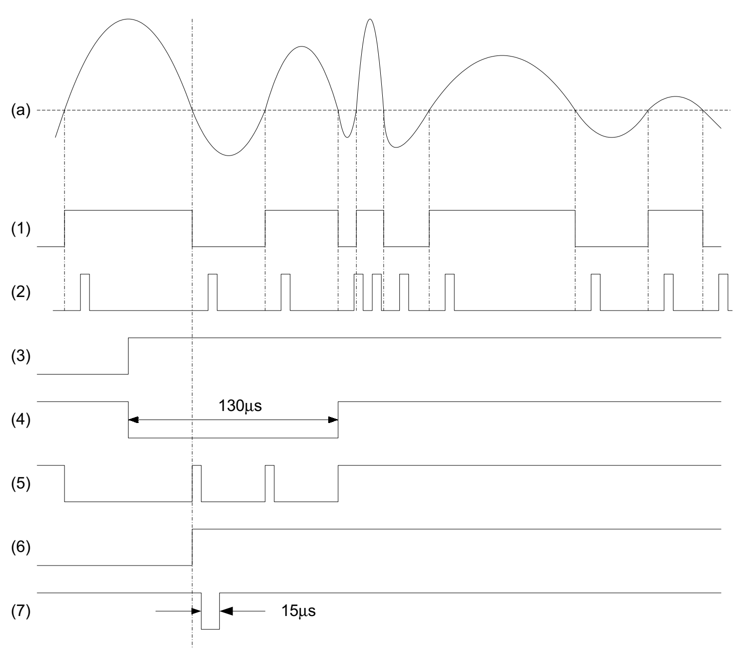


Fig. 6-1-3 Zero Cross Switching Circuit Internal Waveform-1

SECTION 7
MECHACON/SERVO CIRCUIT

7.1 MECHACON/SERVO BLOCK DIAGRAM

7.1.1 CPU system operation block

The CPU system is composed of two CPUs-SYSCON CPU and TIMER CPU as shown in Fig. 7-1-1. Communication is carried out in the same way as currently done using the serial data line, clock line, and chip select line to control the ICs.

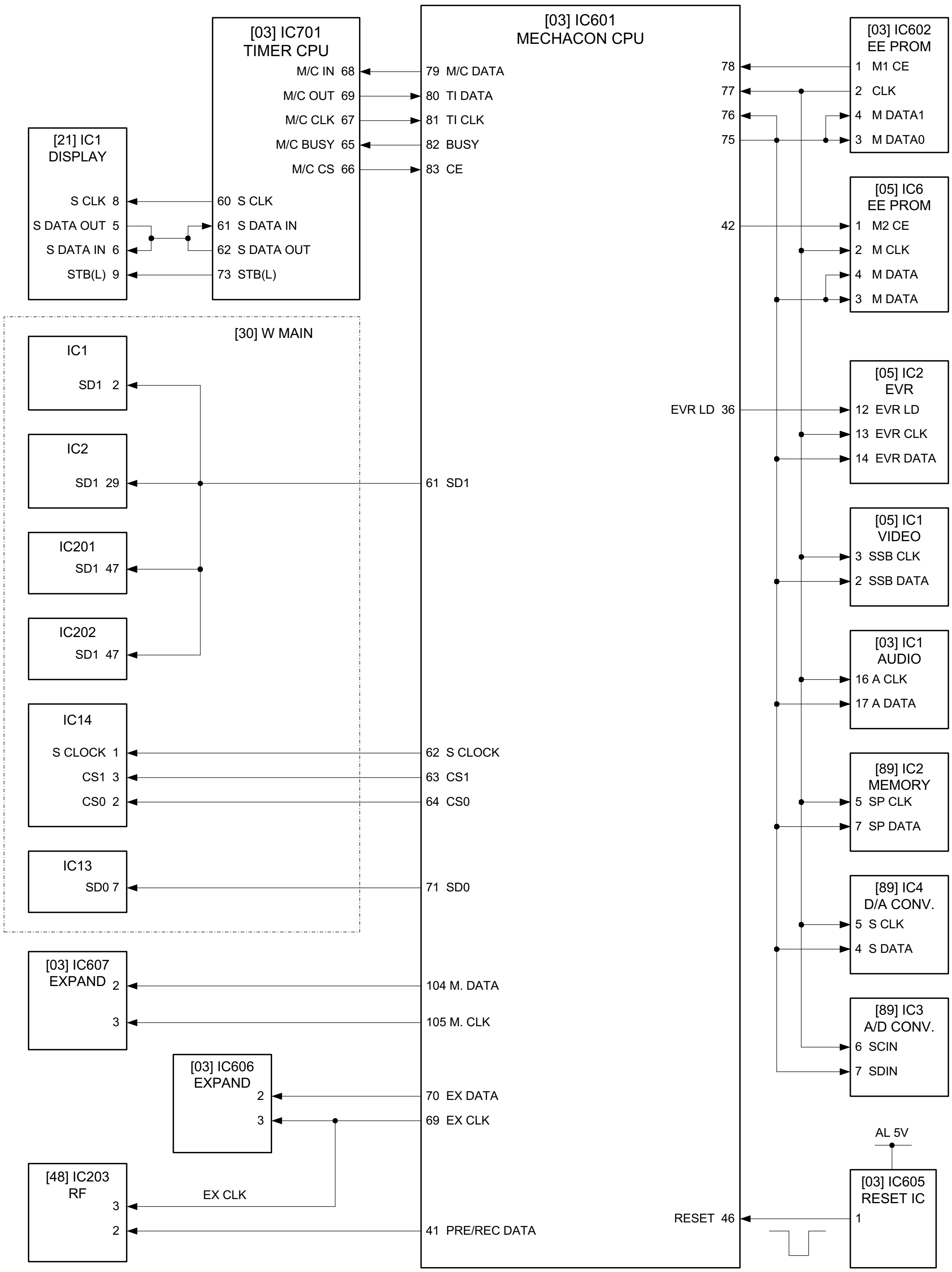


Fig. 7-1-1 CPU System Operation Block

7.1.2 Mechacon/Servo system operations block

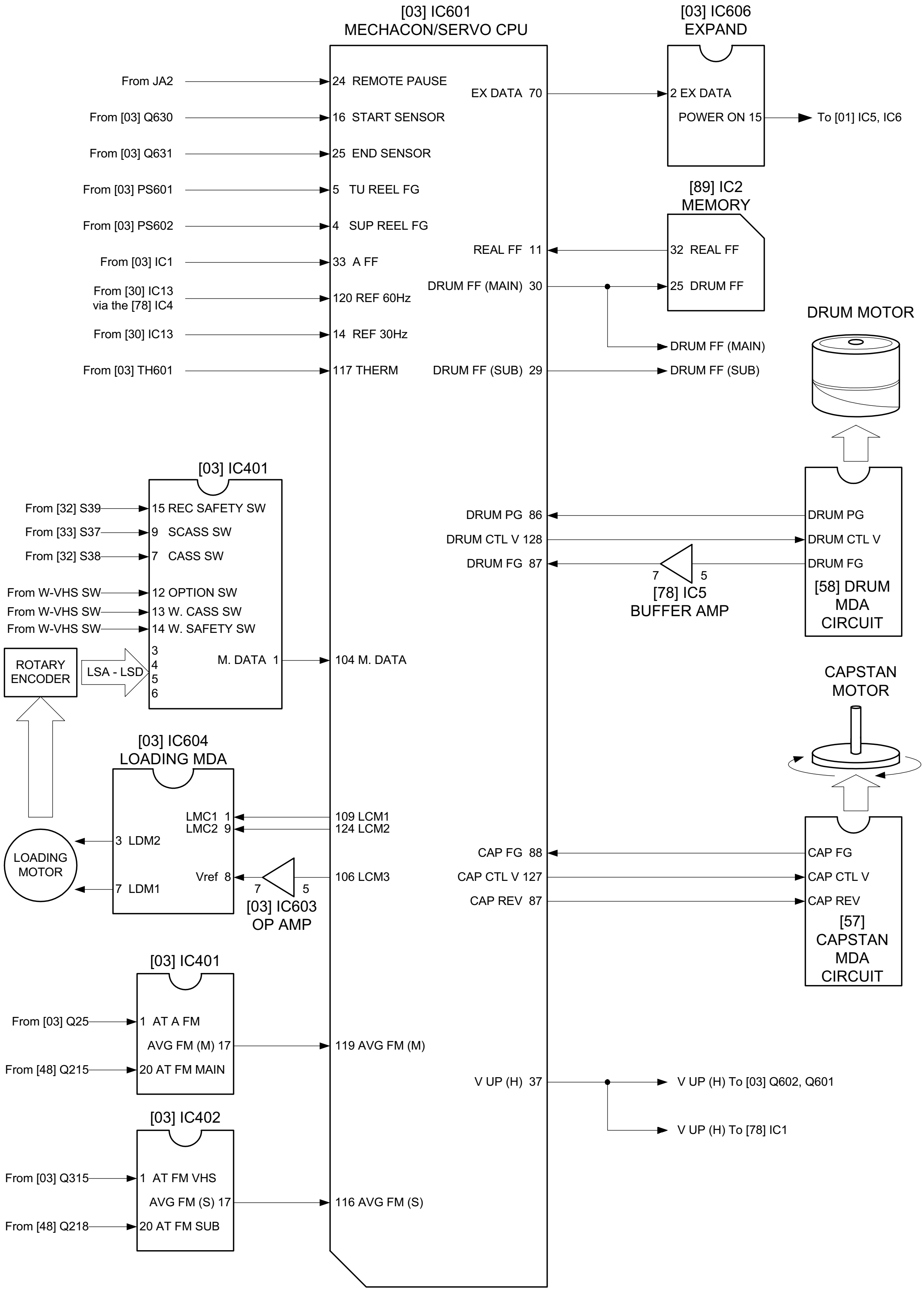


Fig. 7-1-2 Block diagram of Mechacon/Servo block

7.1.3 Doctor System

The doctor system is a system which can solve bugs of the main program written in ROM inside the system controller CPU by adding the doctor data to the EEPROM.
Fig. 7-1-3 shows the block diagram of the doctor system.

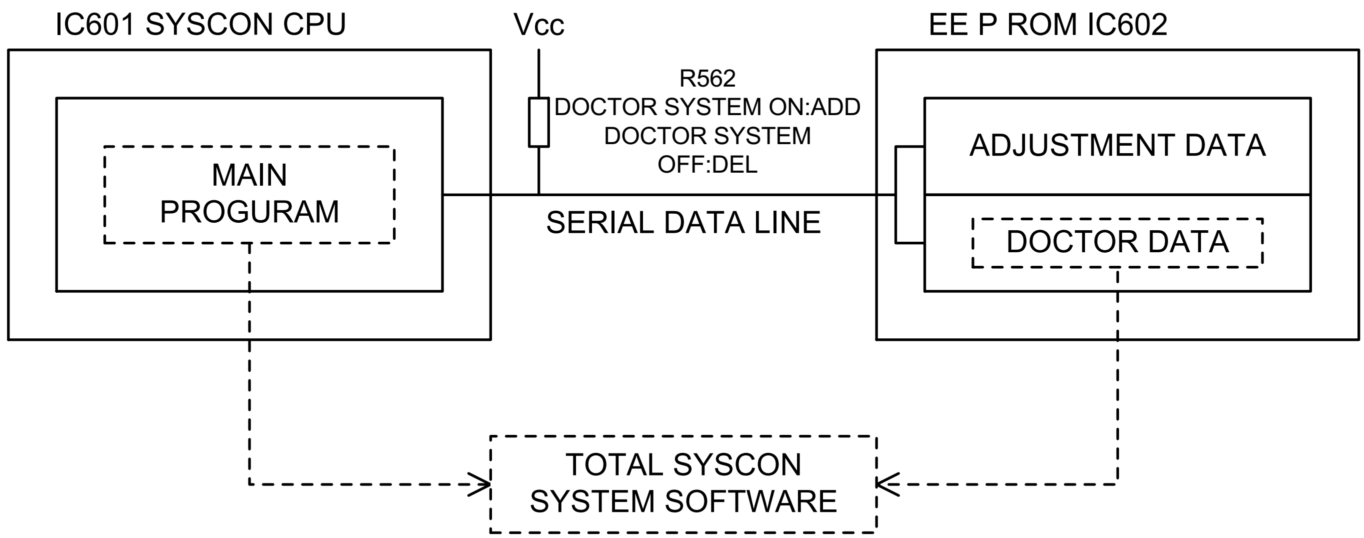


Fig. 7-1-3 Block Diagram of Doctor System

When power is supplied to the system controller system, first before starting the system, the main program checks if the serial data line is pulled up or not.
If the serial data line is pulled up, the main program reads the doctor data into itself. After this, the main program which now incorporates the doctor data starts as the system controller system total program.
If the serial data line is not pulled up. the main program starts directly as the system controller system total program.
This systems works for bugs, and should be handled carefully.
This is because if the three elements-main program version, doctor data version, and doctor system ON/OFF setting do not corresponding, the system controller system total program overruns.
Consequently, when replacing the system controller CPU and EEPROM, make sure that the three elements-main program version, doctor system ON/OFF setting, and doctor data version match.

7.2 MECHACON CPU FUNCTION
7.2.1 Mechacon CPU IC601 pin function
1. IC601 pin functions table (1/3)

Pin No.	Label	In/Out	Description
1	Vcc	-	System power
2	CAP REV (L)	Out	Capstan motor reverse control (REV: L)
3	GND	-	Ground
4	SP FG	In	Supply reel FG input
5	TU FG	In	Take-up reel FG input
6	BS MUTE/F. ERR	In/Out	BS mute mode: L
7	BS CLK	Out	Clock for BS tuner
8	CPST	Out	Strobe signal output for BS data transmission
9	CONW	In	Control code (16 bits) after descrambling and charged flag (4 bits) signal input
10	Vss	-	Ground
11	REAL FF	In	Drum motor rotation detection/recording editing timing control
12	BIT IN (H)	In	Bit stream detection (internal/external switching, P. OFF: Through)
13	MUSE (H)	In	MUSE broadcast detection (MUSE: H)
14	REF 30	In	Reference signal switching (30 Hz)
15	A/M/S	Out	Head select (PB: H/SP BEST SEARCH: M/STILL: L)
16	START SENSOR	In	Start sensor/leader tape detection (detected: L)
17	Hi-Fi REC ST (L)	Out	Hi-Fi sound recording start
18	FLYING ERASE ON (H)	Out	Flying erase head control (ON: H)
19	REC CTL OUT	Out	Control pulse output for recording
20	SYNC DET	In	Detection of presence/absence of SYNC signal when ground broadcasts are received
21	DET S (H)	In	Differention of VHS/S-VHS during playback
22	SERVICE	In	Mchanism service mode
23	TEST	-	Not used
24	REMOTE PAUSE	In	Remote pause control (PAUSE: ON: L)
25	END SENSOR	In	End sensor/trailer tape detection (detected: L)
26	NOISE DET (L)	In	HI-Fi audio recording detection (Noise detected: L)
27	HEAD SELECT	Out	Head select (EP head: H/SP head: L)
28	V. PULSE	Out	V. pulse output (video mute: L)
29	D. FF (S)	Out	Drum FF output (SUB)
30	D. FF (M)	Out	Drum FF output (MAIN)
31	HD. DET (L)	In	HD detection (HD detected: H)
32	REC ST (H)	Out	Video recording start: H
33	A. FF	Out	Audio FF output
34	VP REF	Out	V. pulse output, V compensation during special playback
35	Vcc	-	System power
36	EVR LD	Out	EVR IC rach signal
37	V. UP (H)	Out	Capstan motor control voltage (voltage up: H)
38	SLOW PULSE	Out	Slow pulse output
39	TRICK (H)	Out	Special playback (Slow/Still: H)
40	P. ROLL OUT	Out	Pre roll singal output
41	P/R DATA	Out	RF control data output
42	M2CE	Out	EEPROM chip enable signal output for VIDEO EVR
43	P. MUTE (H)	Out	Picture mute control (Mute ON: H)
44	NUA	-	Not used
45	NUB	-	Not used
46	RESET	In	CPU reset terminal (RESET ON: L)
47	X IN	In	Main system clock
48	X OUT	Out	Main system clock
49	CLK SEL	-	5V
50	Vss	-	Ground

Table 7-2-1 IC601 pin function (1/3)

•IC601 pin functions table (2/3)

Pin No.	Label	In/Out	Description
51	XC IN	-	Not used
52	XC OUT	-	Not used
53	S MODE	Out	Address data for W circuit
54	WA OUT	Out	Wide aspect mode: L
55	A. REC (H)	In	Audio recording mode: H
56	MAIN (L)/STEREO (H)	Out	Voice multiplexed broadcast reception (Main audio: L/stereo: H)
57	TU DATA	Out	Tuning data output
58	TU MUTE (H)	Out	Tuner mute control (Mute: H)
59	TU CLK	Out	Clock for data transfer to tuner unit
60	VIDEO (L)	-	Not used
61	S. D1	Out	Data 1 for W ciruict
62	S. CLK	Out	Clock for W ciruict
63	CS1	Out	Chip select 1
64	CS0	Out	Chip select 0
65	A EVR (L)	Out	Audio EVR mode: L
66	A MUTE (H)	Out	Audio mute mode: H
67	FULL ERASE ON (H)	Out	Control signal output for full erase head (Erase ON: H)
68	-	-	Not used
69	EX CLK	Out	Clock for expander IC
70	EX DATA	Out	Data for expander IC
71	SD0	In	Data 0 for W circuit
72	EE (L)	Out	EE mode: L
73	MOVE	Out	Slow pulse output for W circuit
74	Vss	-	Ground
75	DATA O	Out	Data output for EE PROM
76	DATA IN	In	Data input for EE PROM
77	M1 CLK	Out	Serial data transmission clock for EE PROM
78	M1 CE	Out	Chip enable signal output for EE PROM
79	M/C DATA	Out	Serial data transfer output for timer CPU
80	TI DATA	In	Serial data transfer input for timer CPU
81	TI CLK	In	Seral data transmission clock for timer CPU
82	BUSY	Out	Data transfer enable for timer CPU
83	CE	Out	Chip enable signal output for timer CPU
84	Vcc	-	System power
85	AMP Vcc	-	Power supply for built-in amp.
86	D. PG	In	Drum PG input
87	D. FG	In	Drum FG input
88	C. FG	In	Capstan FG input
89	AMP Vref	-	Reference voltage for built-in amp.
90	-	-	Not used
91	PB CTL P	In	Control pulse input
92	-	-	Not used
93	-	-	Not used
94	-	-	Not used
95	-	-	Not used
96	-	-	Not used
97	-	-	Not used
98	-	-	Not used
99	CTL Vss	-	Ground
100	AMP Vss	-	Ground

Table 7-2-1 IC601 pin function (2/3)

•IC601 pin functions table (3/3)

Pin No.	Label	In/Out	Description
101	AVcc	-	System power for analog ciruciut
102	Vref	-	Reference voltage for analog ciruciut
103	Vss	-	Ground
104	M. DATA	Out	Serial data output for expander IC
105	M. CLK	Out	Serial data transmission clock for expander IC
106	LCM3	Out	Mode motor drive voltage control 3
107	REV (L)	Out	Reverse mode: L
108	SLOW CTL P (H)	Out	Control pulse switching signal (SLOW/STILL: H)
109	LCM1	Out	Model motor drive voltage control 1
110	S CURVE IN	In	AFC control data/tuning detected
111	PROTECT	In	SWD 5V/12V detected (for emergency)
112	BS ANT	In	Satellite broadcast reception level detection (AGC AMP output is D/A conreted to DC)
113	BS AFC	In	Data input for satellite broadcast AFC control
114	TU LED	Out	Ground broadcast stereo display LED switching signal
115	DEW SENSOR	In	Dew sensor data input
116	AVG FM (S)	In	Auto tracking data input (HD SUB)
117	THERM	In	Thermal correction detect (capstan slow brake timing control)
118	WA LEVEL	In	Wide aspect detect (full mode input detected)
119	AVG FM (M)	In	Auto tracking data input (HD MAIN, SD, S-VHS, VHS)
120	REF 60	In	Reference signal input (60 Hz)
121	INDEX (H)	Out	Index signal writing control/index signal detection (index ON: H)
122	BS CE	Out	BS data chip enable
123	V. FM (H)	Out	PB FM signal switchig of auto tracking (video FM: H)
124	LCM2	Out	Mode motor drive voltage control 2
125	BS DATA/CPDA	Out	BS tuning data/control data
126	BS TH (L)	Out	BS through mode: L
127	CAP CTL V	Out	Capstan motor rotation control voltage output
128	DRUM CTL V	Out	Drum motor rotation control voltage output

Table 7-2-1 IC601 pin function (3/3)

7.2.2 IC601 pin assignment

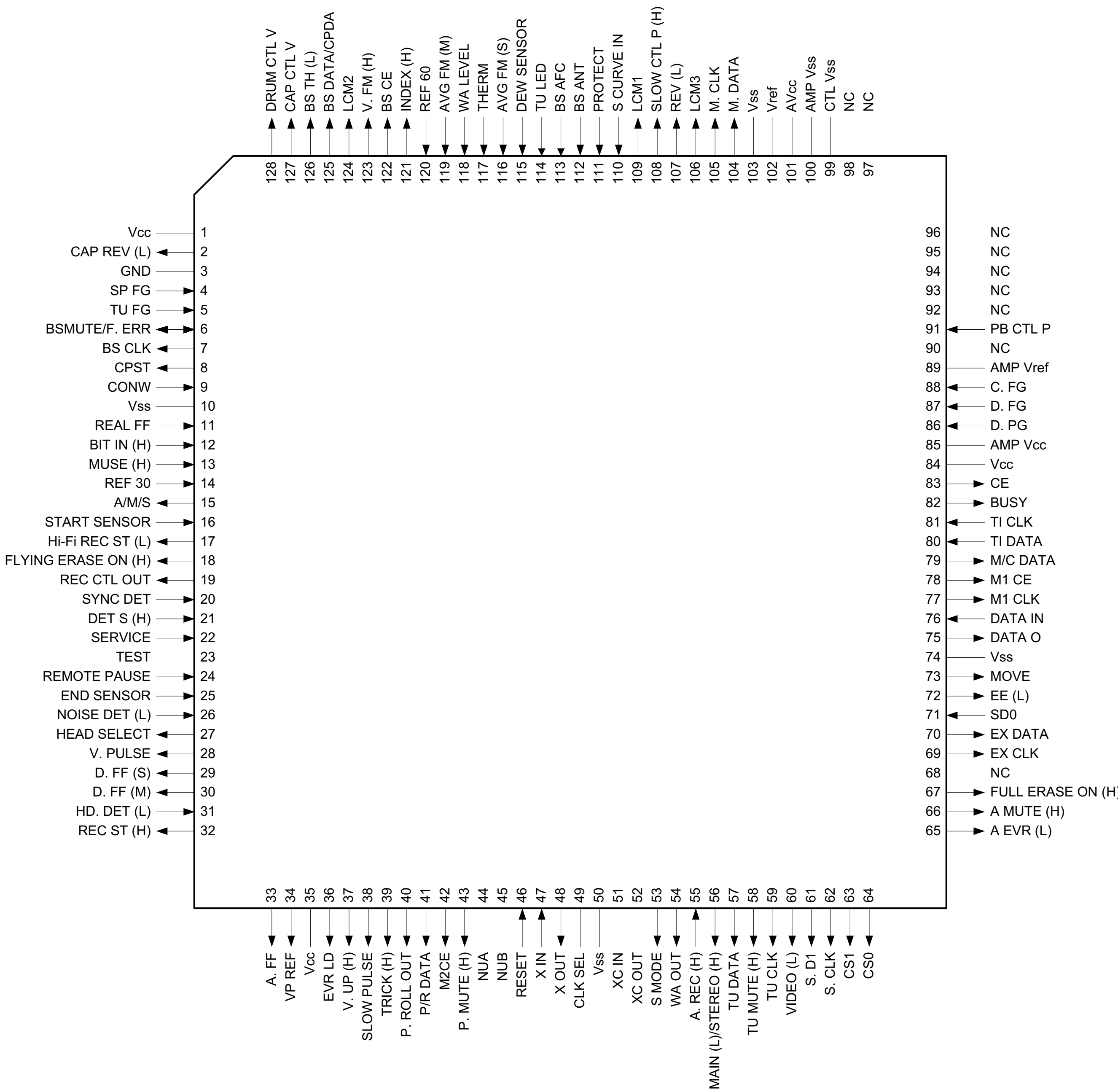


Fig. 7-2-1 IC601 pin assignment

SECTION 8
SWITCHING REGULATOR CIRCUIT

8.1 BASIC OPERATIONS OF PWB TYPE SW. REG CIRCUIT

The schematic diagram shown in Fig. 8-1-1 is a wiring diagram of the power supply circuit. This power supply circuit adopts a method called PWB type switching regulator.
Amongst its features, the changes of the output voltage of the secondary side are fed back to the primary side to control the oscillation duty ratio of the primary side and change the energy transmitted to the secondary side in order to stabilize the output voltage of the secondary side.

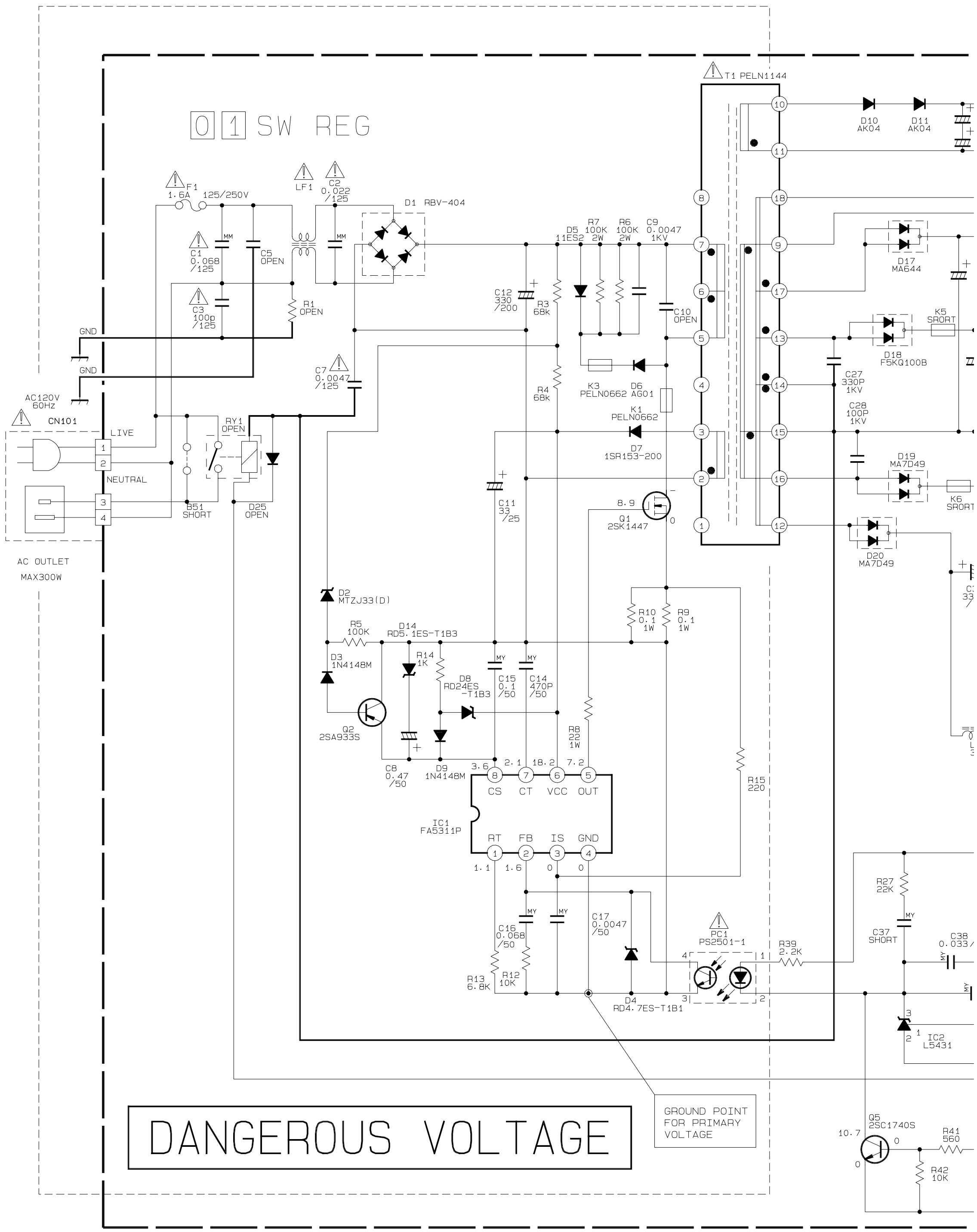


Fig. 8-1-1 Switching regulator circuit diagram (1/2)

In this circuit, the changes in the M12V output voltage of the secondary side are fed back to the primary side. Normally, the specifications of the output voltage are harsh, and feed back is imposed using outputs with considerable load. In this case, by stabilizing the output voltage, the other output voltages also stabilize automatically.
The following describes how this circuit is subject to feed back when the M12V output voltage changes due to the change of the load.

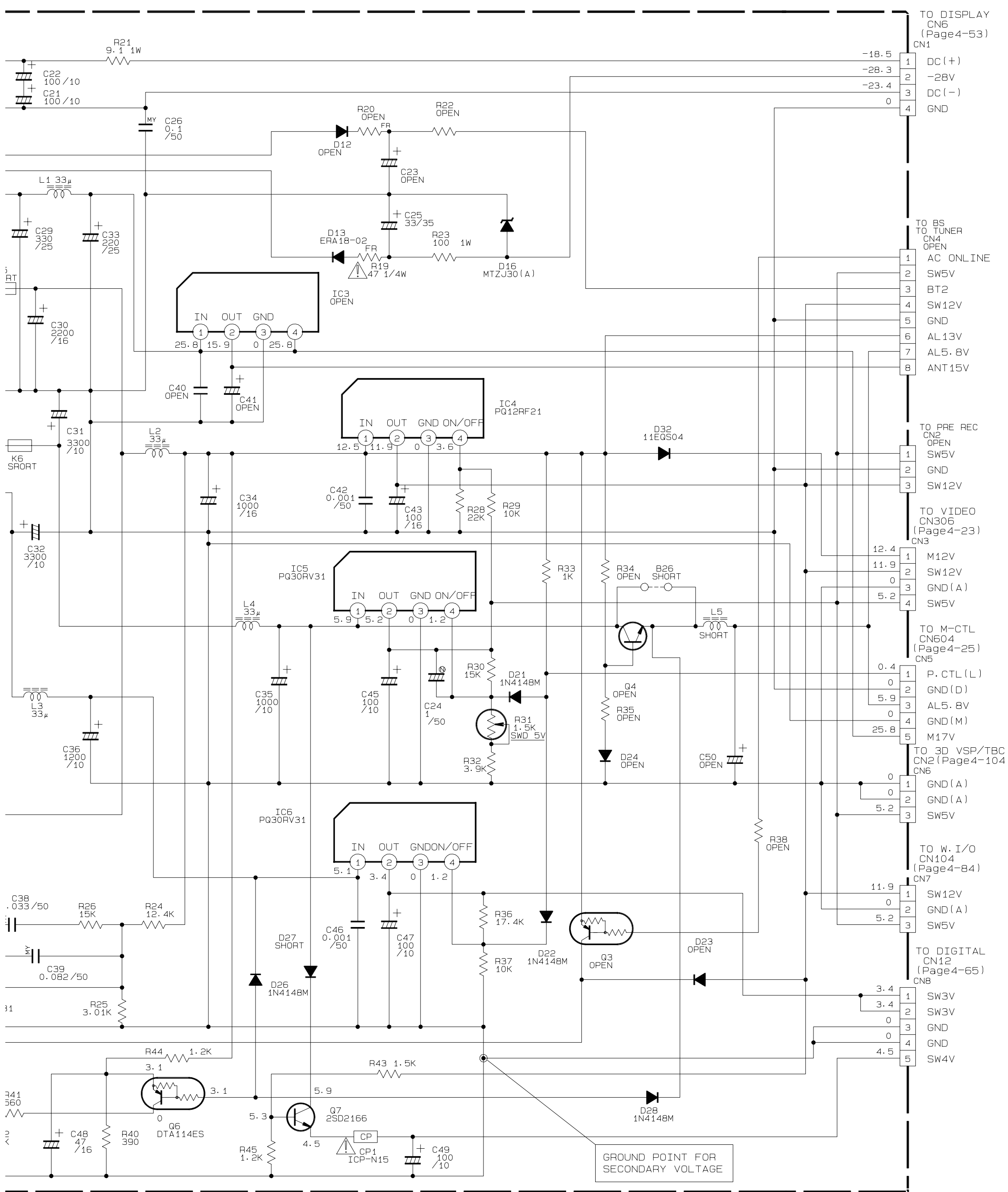


Fig. 8-1-1 Switching regulator circuit diagram (2/2)

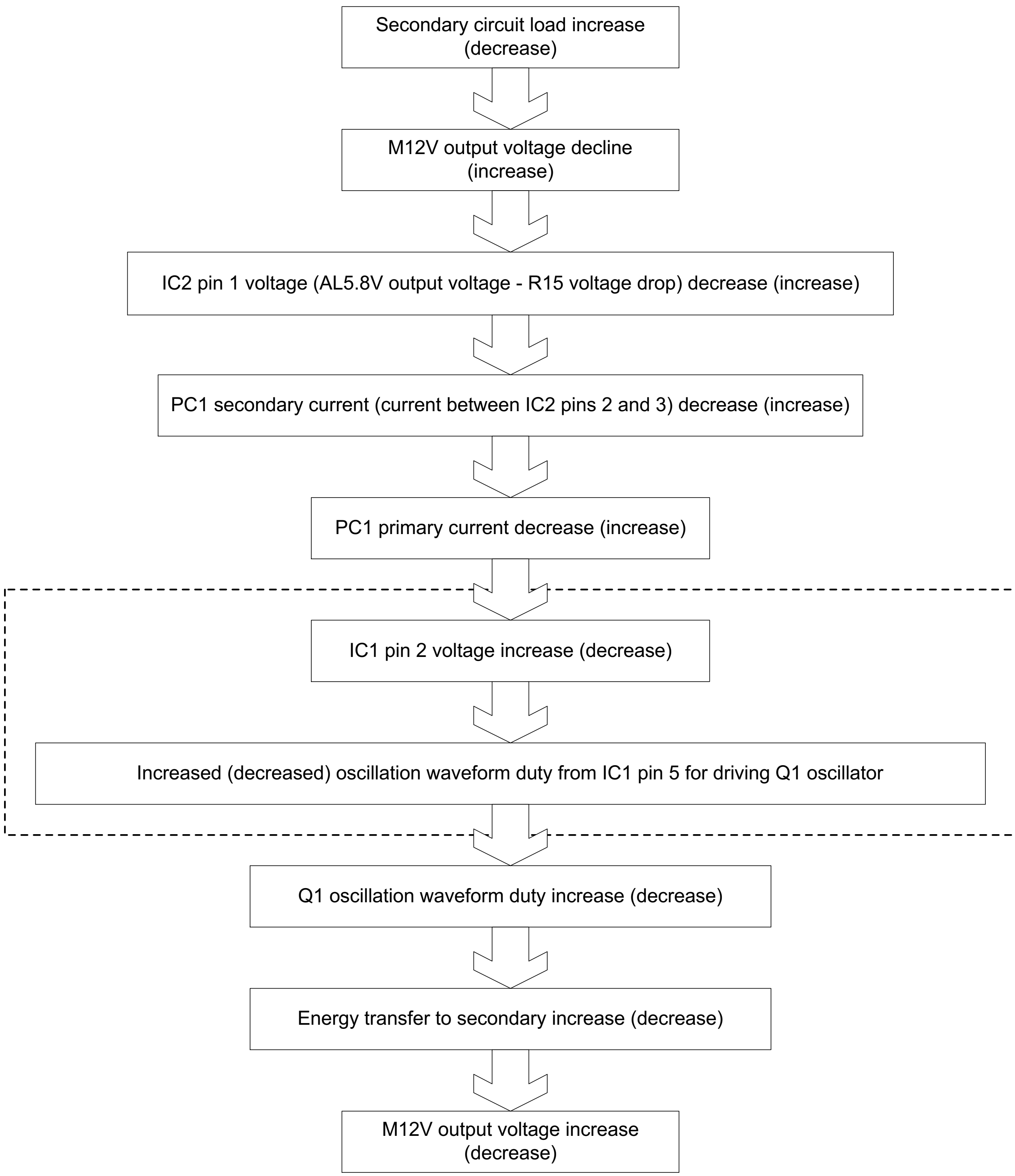


Fig. 8-1-2 Switching regualtor feed back flow chart

8.2 BASIC OPERATIONS FOR OSCILLATION CONTROL (IC1)

Details of the operations of IC1 (portion enclosed in dotted lines in Fig. 8-1-2) are explained below.
Fig. 8-2-1 shows the block diagram of the internal and peripheral circuits of IC1 while Table 8-2-1 shows the pin table of IC1.

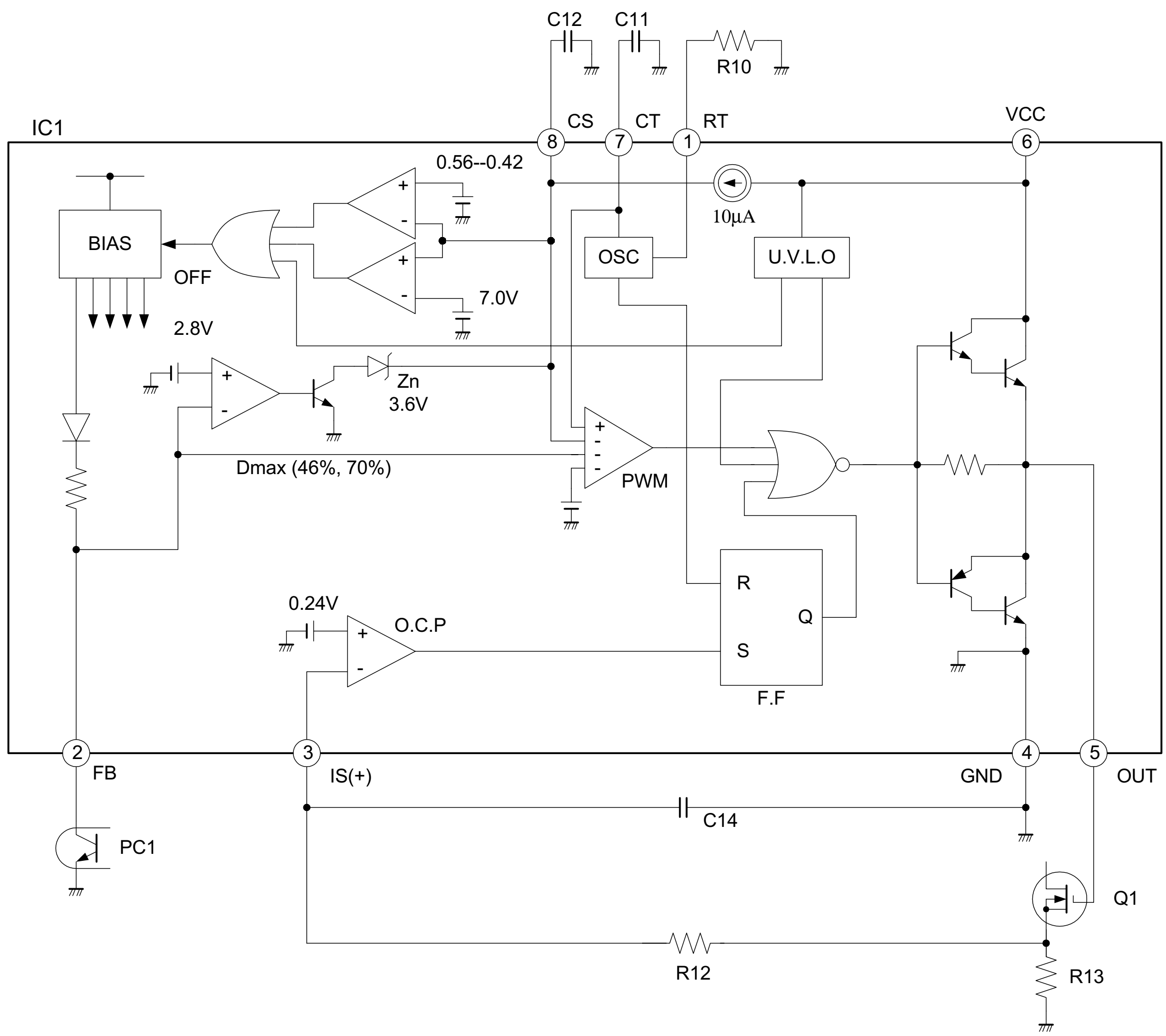


Fig. 8-2-1 Block diagram of the internal and peripheral circuits of IC1

Pin No.	Label	Description
1	RT	OSC timing register
2	FB	Feed back terminal
3	IS(+)	Overcurrent (+) terminal
4	GND	Ground
5	OUT	Output – 1 –
6	VCC	Power supply
7	CT	OSC timing capacitor
8	CS	Soft start, ON/OFF control

Table 8-2-1 Pin function table of IC1

The PWM comparator determines the duty ratio of the primary side oscillation waveform. The output of the PWM comparator is inverted, amplified, output from the OUT terminal to drive the Q1 oscillator.
Fig. 8-2-2 shows an enlargement of this portion.
Fig. 8-2-3 shows the timing chart of the PWM comparator.

The PWM comparator has four inputs.
The generator output voltage determining the generating frequency (the generating frequency is determined by the constants of the resistor connected to the RT terminal and capacitor connected to the CT terminal) is compared with the CS (soft start) terminal voltage, FB (feed back) terminal voltage, and DT (reference) voltage. Amongst the CS terminal voltage, FB terminal voltage, and DT voltage, the lowest voltage is given the priority, and compared with the generator output voltage. As shown in Fig. 8-2-3, which voltage (CS terminal voltage, FB terminal voltage, and DT voltage) is the lowest depends on the status of this circuit.
As the CS terminal voltage rises gradually from the starting point of oscillation due to the charging of C15 connected to the CS terminal, it determines the duty ratio of the oscillation waveform of the starting point of the oscillation. In other words, this prevents the sudden rising of the oscillation waveform.
The FB terminal voltage gradually drops from the level of the bias voltage from the starting point of the oscillation, and the duty ratio of the oscillation waveform is determined at the point it is smaller than the CS terminal voltage. In other words, it determines the duty ratio of the oscillation waveform during normal operations.
The DT voltage does not change according to the status of the circuit as it is the reference voltage.
This voltage sets the maximum duty ratio of the oscillation waveform.
No matter how much the CS terminal voltage and FB terminal voltage rise according to the status of the circuit, the duty ratio of the oscillation waveform will not be greater than the maximum duty ratio set by the DT voltage.

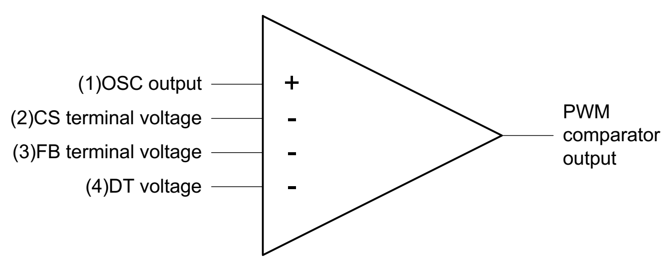


Fig. 8-2-2 Enlargement circuit

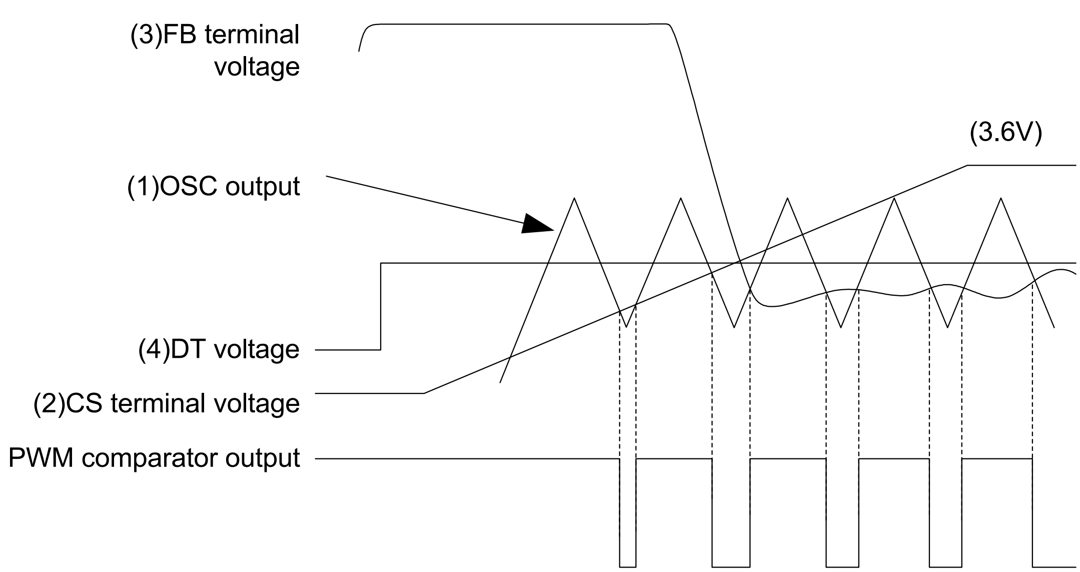


Fig. 8-2-3 Timing chart of the PWM comparator

8.3 VARIOUS PROTECTION SYSTEMS OF THE PWM TYPE SW. REG CIRCUIT

8.3.1 Secondary side circuit load protection system

When the secondary side circuit becomes overloaded due to some reason and the M12V output voltage lowers, the FB terminal voltage of IC1 rises as described in the flowchart shown in Fig. 8-1-2. When this voltage exceeds the reference voltage (2.8V) of the comparator C3 of Fig. 8-2-1, the output of C3 becomes LOW, and the transistor Q becomes OFF. At this time, the CS terminal voltage clamped at 3.6V is unclamped by the Zener diode Zn, charging is further performed by the rated power supply (10μA), and the CS terminal voltage
rises. When this CS terminal voltage exceeds the reference voltage of the comparator C2, the output voltage of C2 becomes HIGH and turns OFF the BIAS circuit. AS a result, IC1 sets into the OFF latch mode, the voltage of the OUT terminal of IC1 is fixed at LOW, and the oscillation of the circuit is stopped.
Fig. 8-3-1 shows the timing chart of this operation.
The current consumed in the OFF latch mode of IC1 is 400 μA (Vcc=9V), and must be supplied via the start resistor. At this time, IC1 automatically discharges the electric charge accumulated in the Q1 gate.
Resetting of this system is performed by setting the power supply voltage Vcc to less than 8.7V or by setting the CS terminal voltage to less than 7.0V forcibly.

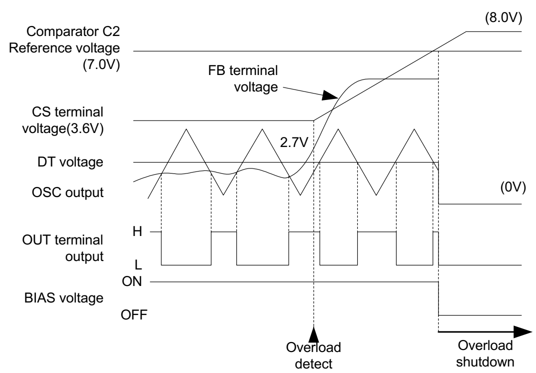


Fig. 8-3-1 Overload protection timing chart

8.3.2 Secondary side overvoltage protection system

When the secondary side output voltage rises due to some reason and the -28V output voltage exceeds the value set, D16 short-circuits and the load rises suddenly. As a result, the above secondary side overload protection system starts operating, and stops the oscillation.

8.3.3 Primary side overcurrent protection system

When the IDS peak value of Q1 rises due to some reason, the peak value of the voltage between the two terminals of R9 rises, and when the voltage exceeds the reference voltage (0.24V) of the comparator C4, the C4 output becomes HIGH, and sets the flip flop output Q to HIGH. At that instant, the output becomes OFF, and shuts the current. This flip flop output Q is then reset by the next oscillation cycle, and turns ON again. This operation is repeated, to perform primary side overcurrent protection.
Fig. 8-3-2 shows the timing chart of this operation.

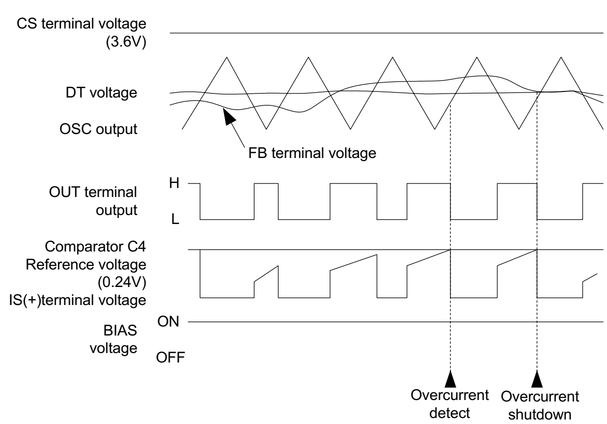


Fig. 8-3-2 Overcurrent protection timing chart

8.4 ESTIMATE OF MALFUNCTION POINTS ACCORDING TO MALFUNCTION SYMPTOMS

The symptoms of malfunctions of this circuit are as follows.

1. The power does not turn ON (the oscillation waveform does not start at all)
In this case, the following malfunction points can be considered.

1) F1 is open.
(Often Q1 will also have short-circuited at the same time.)
2) Q1 has short-circuited.
(Often F1 will be open at the same time.)
3) Q1 is open.
(Often F1 will also be open at the same time.)
4) The parts of the start circuit of R3 and R4, etc. are defective.

In the case of 1), 2), and 3), F1 and Q1 should be replaced at the same time because, as described above, both often damage together, and even if a part is not damaged, it's characteristics and durability would have dropped considerably.

2. The power does not turn ON (The Q1 oscillation waveform starts once but stops immediately)
In this case, the secondary side overload protection system would often will operating. The specific malfunction points which can be considered are as follows.

1) The secondary side overload protection system is operating due to the short-circuit (including other circuits) between the power supply circuit secondary side/load side and GND.
2) Due to the defects of the parts in the feedback loop described in Fig. 8-1-2, the secondary side output voltage has become overvoltage, D16 has short-circuited as a result, and caused the secondary side overvoltage protection system to operate.
3) The secondary side overload protection system is operating due to the defects of the parts in the feedback loop described in Fig. 8-1-2.

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